

MODEL NAME : ZAL00
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WW000 LA-A491P M/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

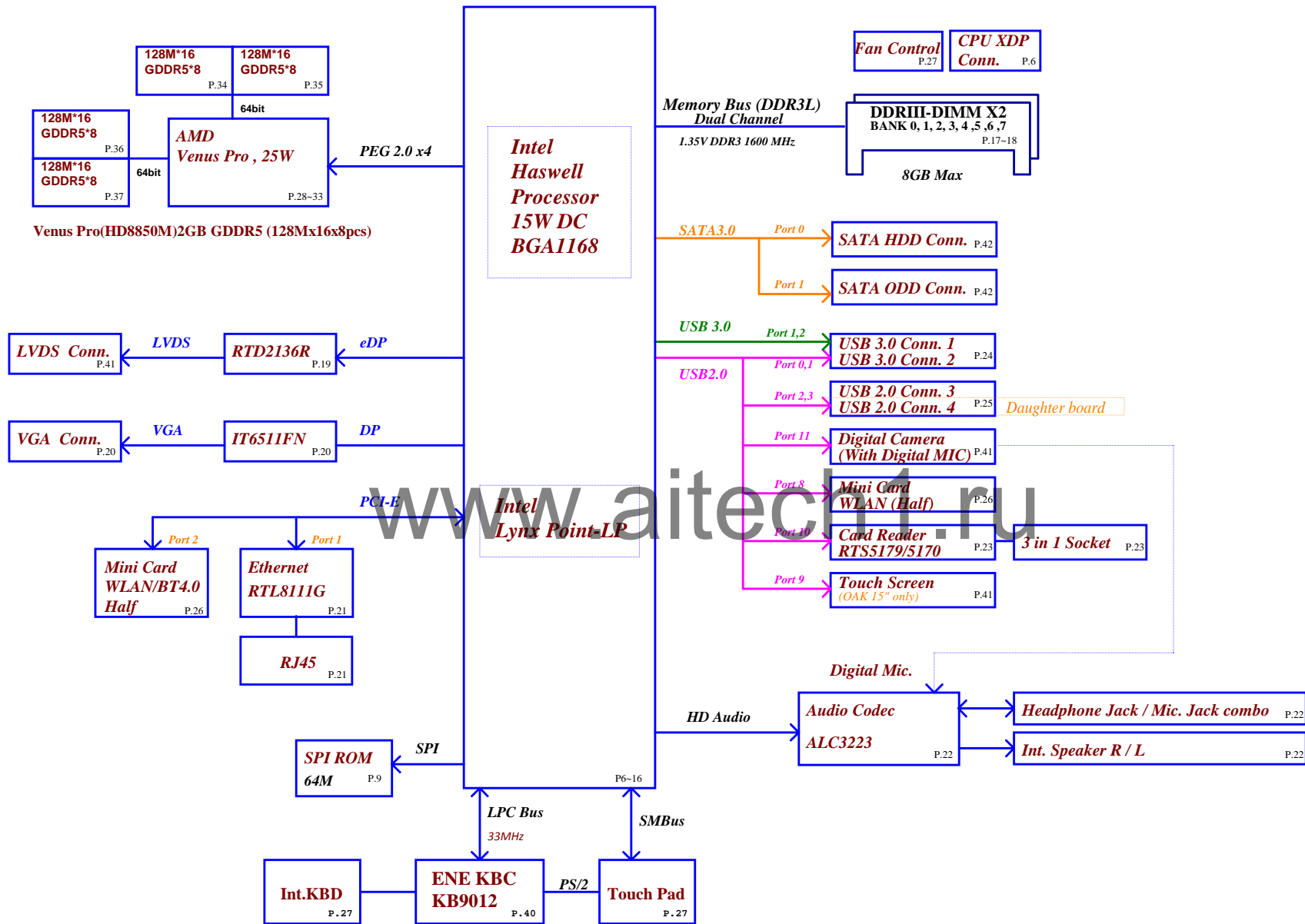
2013-05-15 Rev: 0.3

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

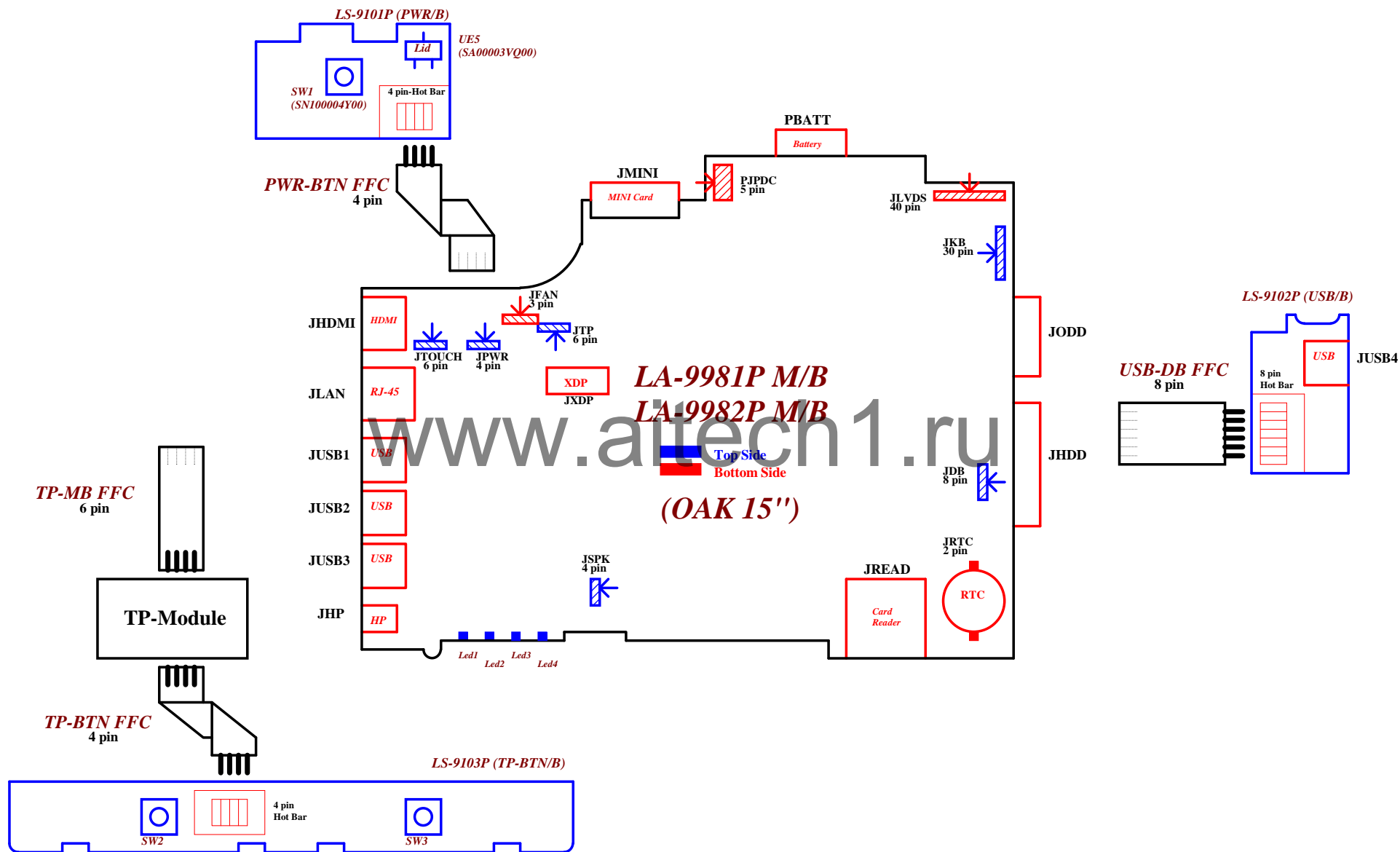
BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS VENUS : VENUS@,DIS@,EMI@,ESD@,RF@,XDP@



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Issued Date	2013/04/01	Deciphered Date	2014/05/01	Title	Cover Page
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Compal Confidential
Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

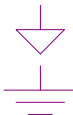
	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

BOARD ID Table

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0
16				

Symbol Note :



: means Digital Ground



: means Analog Ground

CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

USB3.0

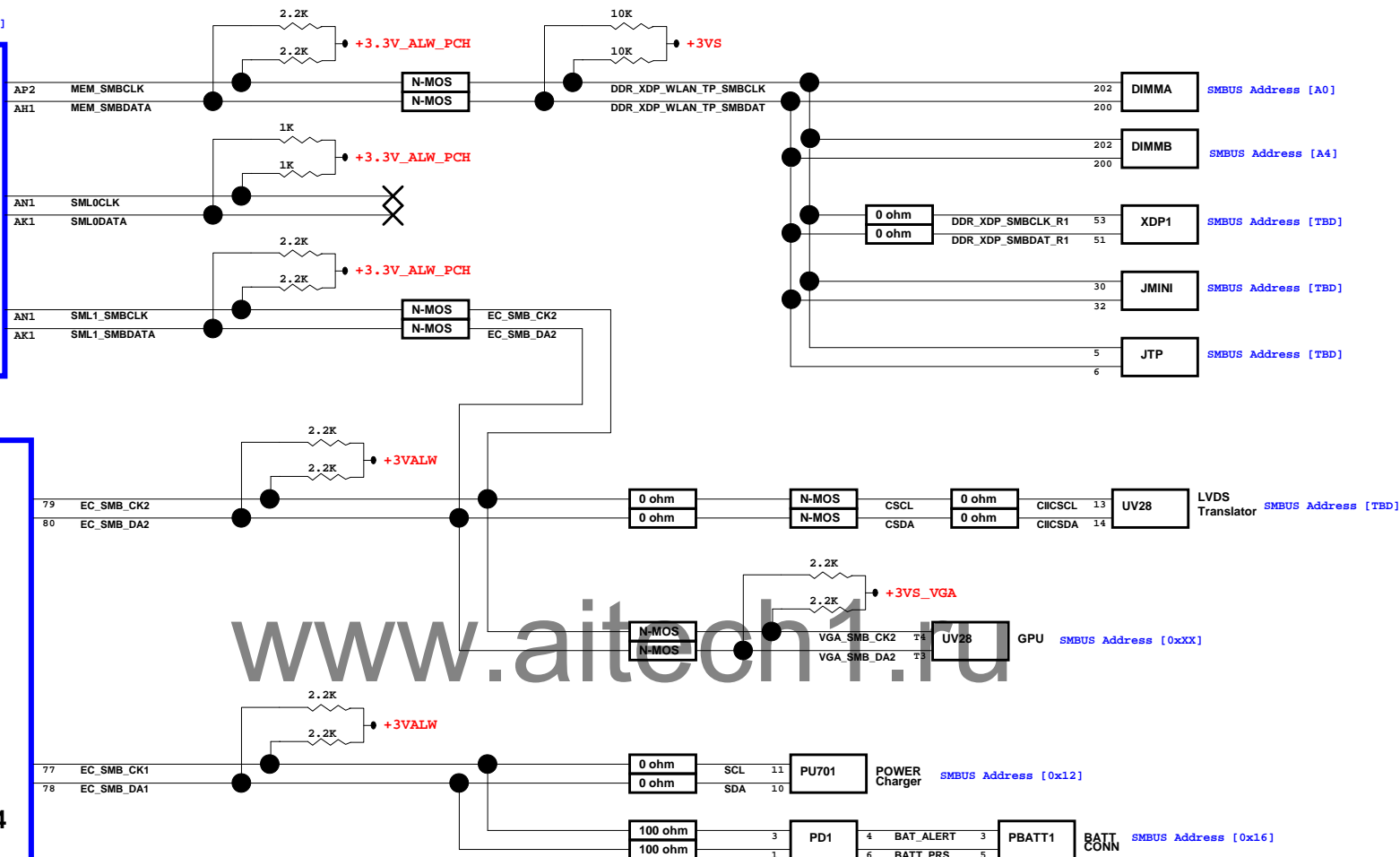
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

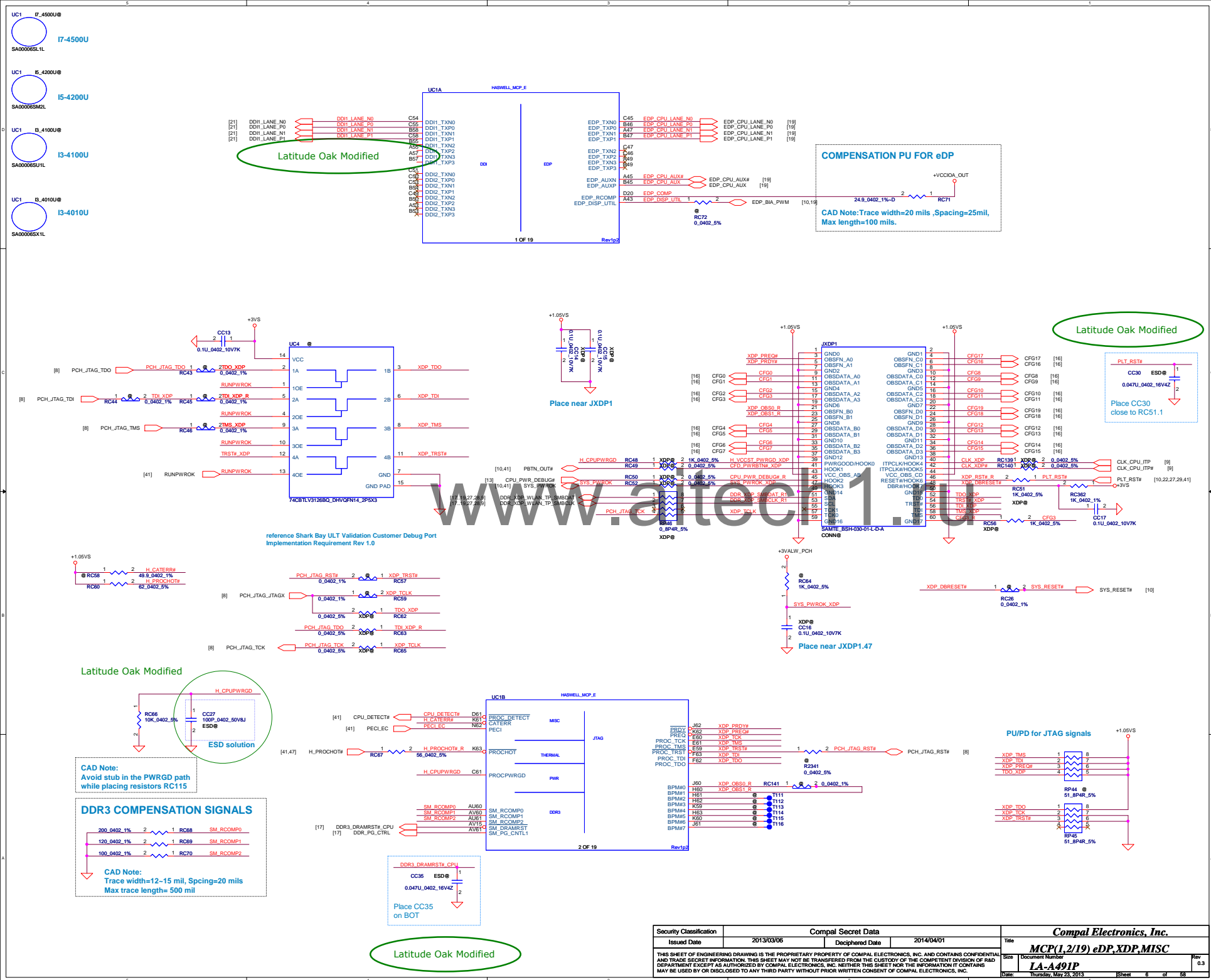
ULT

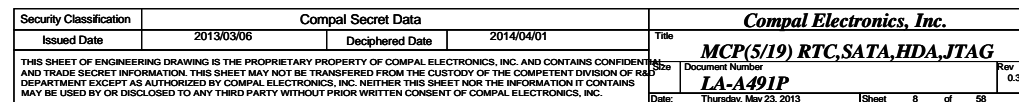
SMBUS Address [0x9a]

MCH
Shark bay

KBC
KB9012A4







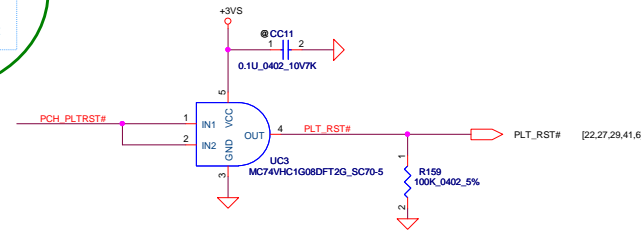
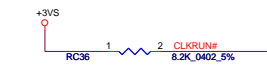
d

PCH_PLTRST#

CC33 ESD0

0.047uF_0402_16V42

Place CC33 close to UC3.1 & UC3.2



DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

CC31 **ESD@**

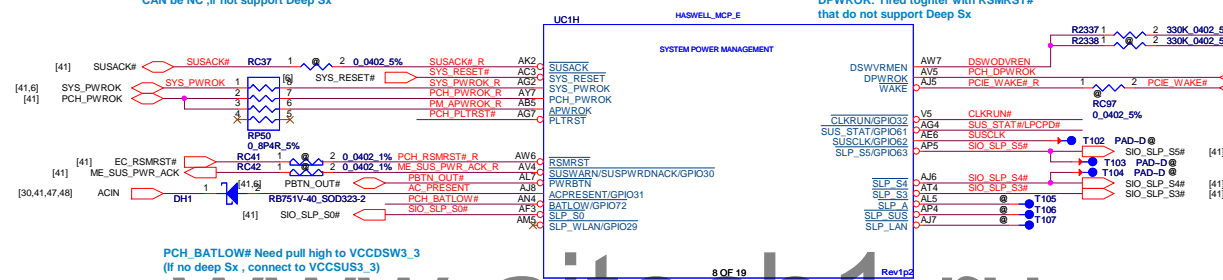
0.047µF 40V 16V42Z

Place CC31 on BOT

CC34 **ESD@**

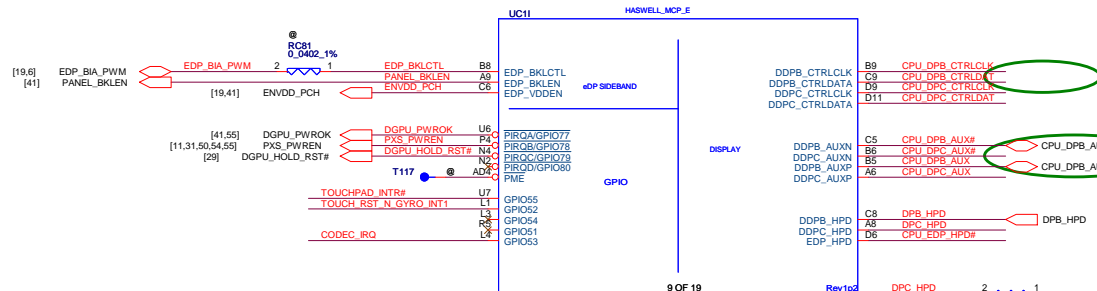
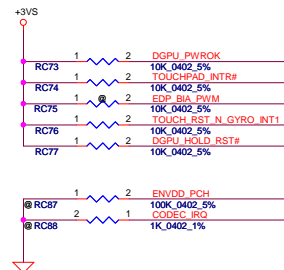
0.047µF 40V 16V42Z

Place CC34 close to RP50.2&RP50.3

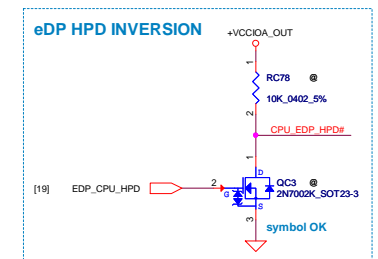


PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)

PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx, connect to VCCSUS3_3)



The diagram shows the internal connections of the RP2040. The CPU is connected to the DPIC via a 2.2k resistor. The DPIC is connected to the RP2040 via a 100k resistor. The RP2040 is connected to the +3V3 supply. The RP2040 is also connected to the ground.



EDP_CPU_HPD 1 RC105 2 CPU_EDP_HPD#
0.0402_5% Reserve for el

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Define EC OD pin. need double confirm.

VR_ON

C96 ESD@

0.1U_0402_10V7K

Place C80 close to R250.1

Figure 10: SVID Alert circuit diagram. The diagram shows a voltage divider circuit. A +1.05V source is connected to a resistor R252 (75_0402_5%). The other end of R252 is connected to a node labeled '2'. This node is also connected to a resistor R254 (43_0402_1%). The other end of R254 is connected to a node labeled '1'. Node '1' is connected to the H_CPU_SVIDALRT# pin. Node '2' is connected to the VR_SVID_ALERT# pin. A note indicates: "Place the PU resistors close to CPU".

**SVID_DAT need to pull-up double side
(PWR_VR & CPU)**

Place the PU resistors close to CPU

R256
130_0402_1%

H. CPU_SVIDDATA

[53] VR_SVID_DATA

```
graph LR
    Vplus[V+] --- R256[R256 130_0402_1%]
    R256 --- Node(( ))
    Node --- R257[R257 0_0402_1%]
    R257 --- VR[VR_SVID_DATA [53]]
    CPU[H. CPU_SVIDDATA] --- Node
```

Signal	Value	Unit	Count
[53] VR_SVID_CLK	0.0402	1%	1
[41,53] VR_ON	0.0402	5%	1
[53] H VR_READY	0.0402	1%	1

[6] CPU_PWR_DEBUG#

RF@
C5212
68P_0402_50V8J

R253
INTEL Check list , XDP use only

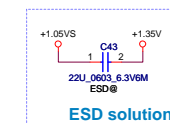
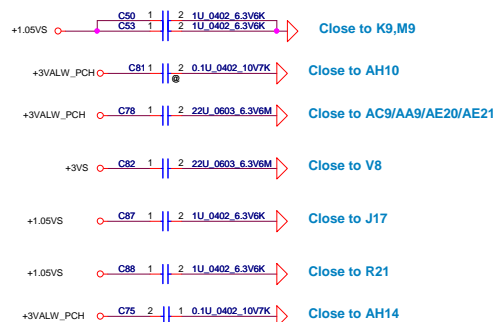
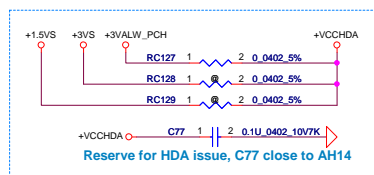
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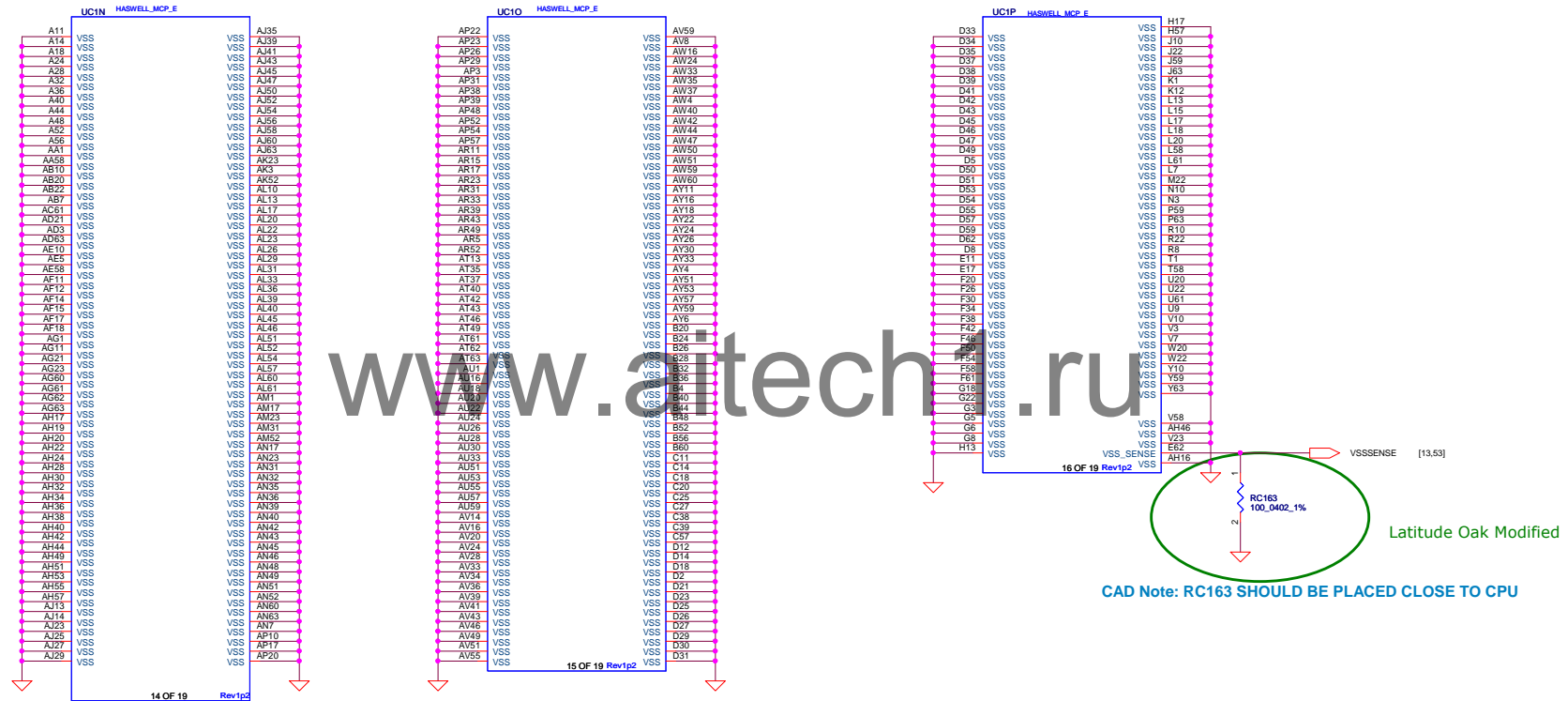
+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

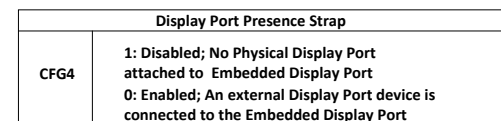
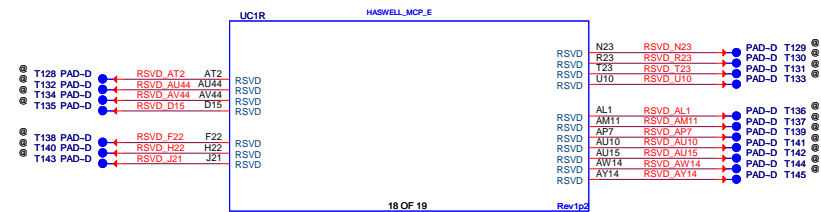
CAD Note: PU resistor on HW side

CAD Note: PD resistor on HW side

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H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

[7] DDR_A_DQS#0..[7]
[7] DDR_A_DQ0..[63]
[7] DDR_A_DQS#0..[7]
[7] DDR_A_MA0..[15]

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

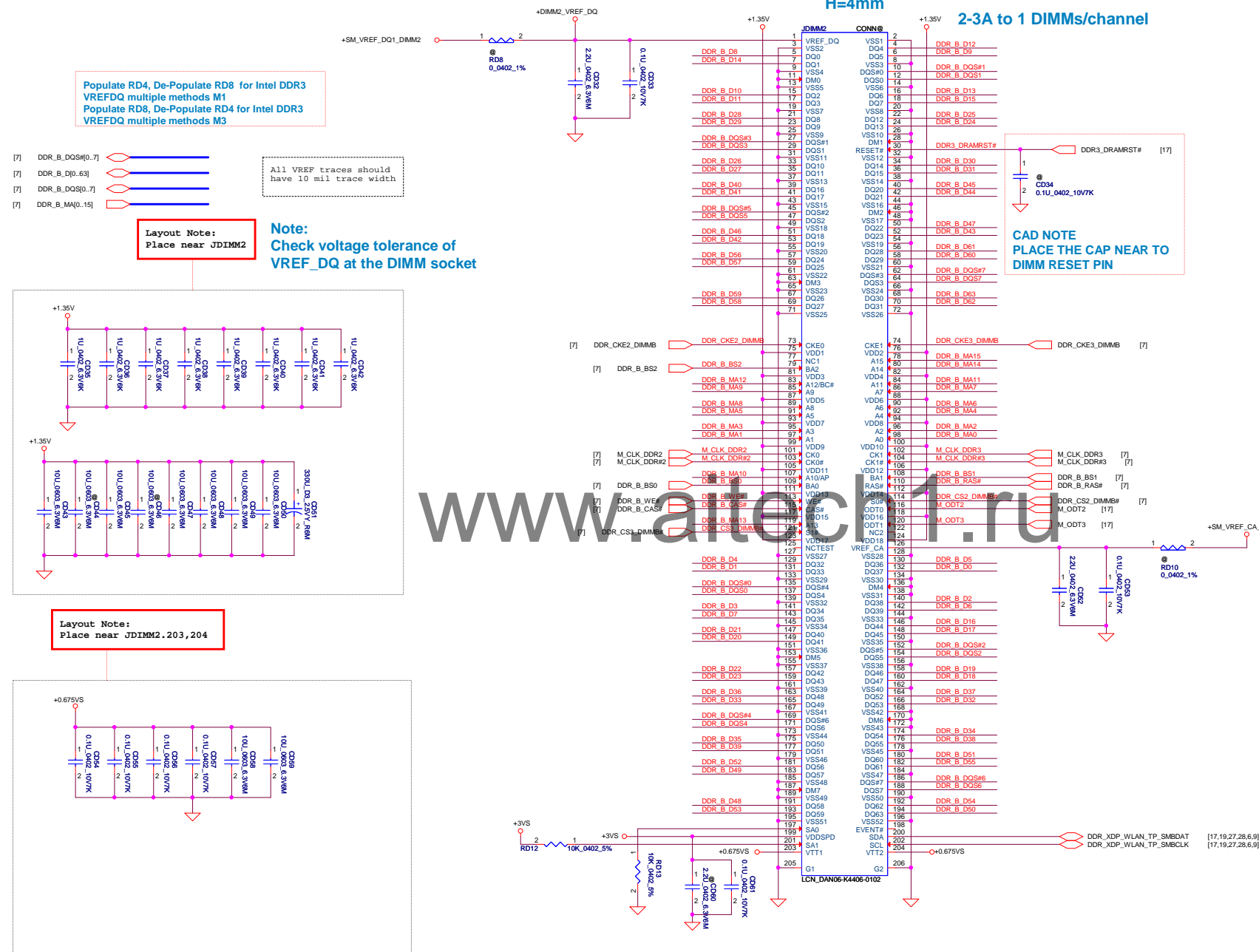
Latitude Oak Modified

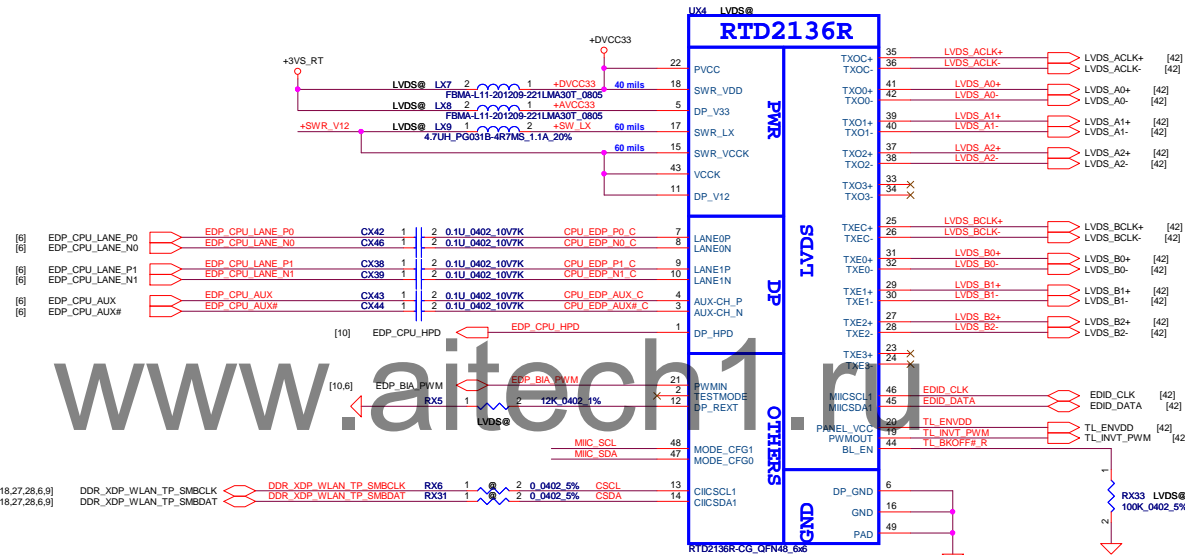
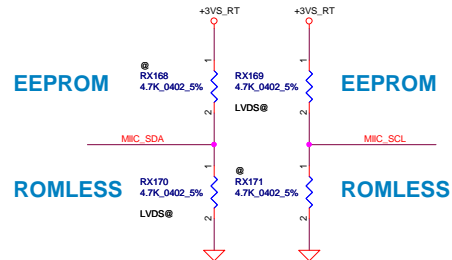
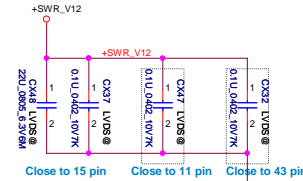
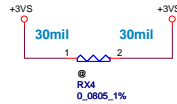
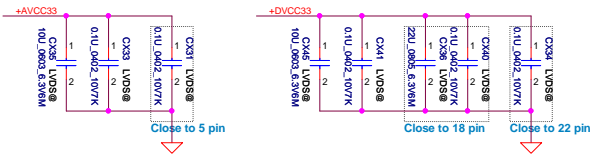
DDR3L SODIMM ODT GENERATION

M_ODT
CD64 ESD@
0.1U_0402_10V7K
Place CC31 between QD2 and R2349

Layout Note:
Place near JDIMM1.203,204

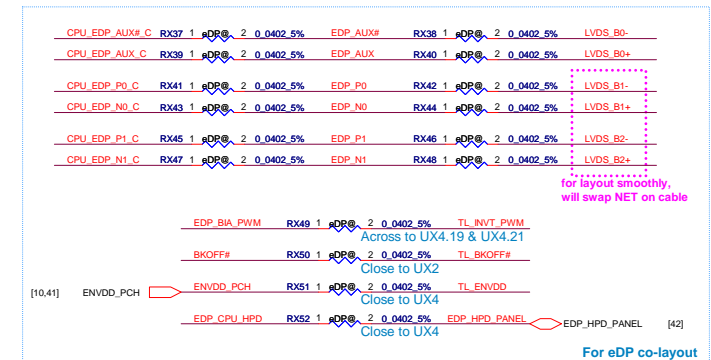
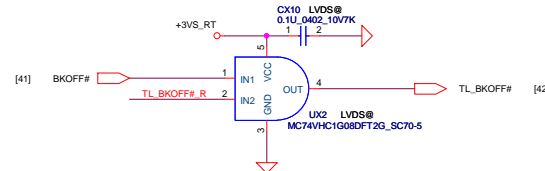
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				DDRIII DIMMA	
				Document Number	
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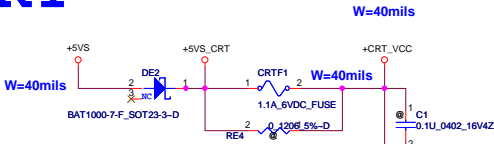



RTD2136S : SA00004NW10
RTD2136R : SA000067100

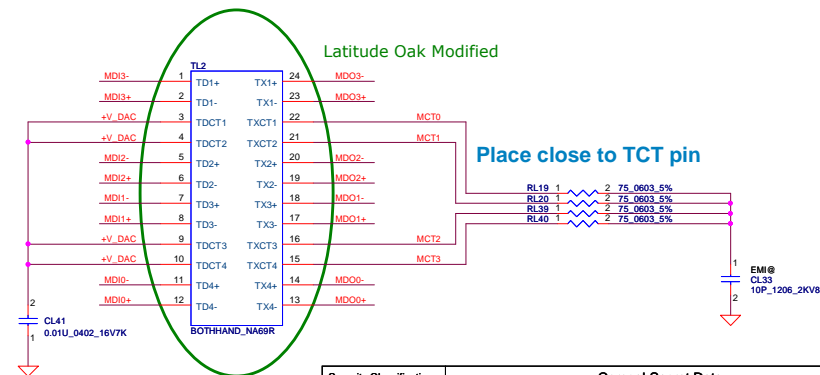
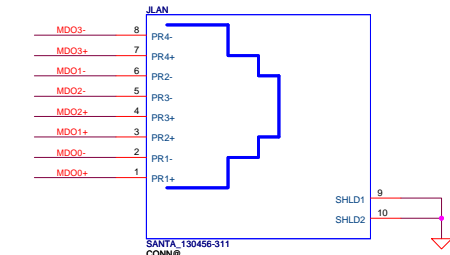
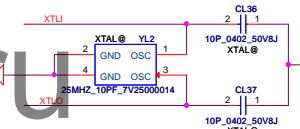
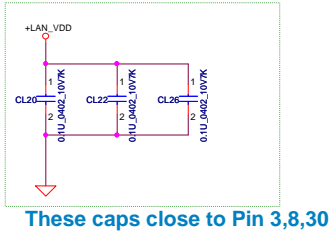
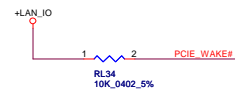
Vendor advise reserve it



tech1.ru



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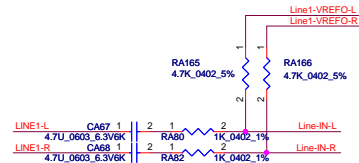
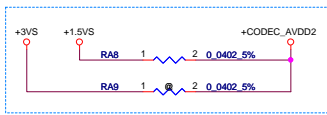
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CA71, CA51 place close to Pin 26

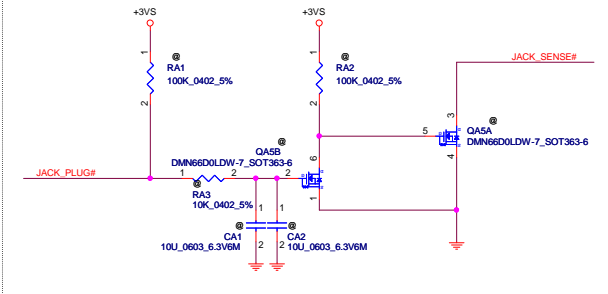
CA53, CA55 change Value
from 100U_0603_6.3V6K to
4.7U_0603_6.3V6K

CA57, CA58 close
to UA1 pin1

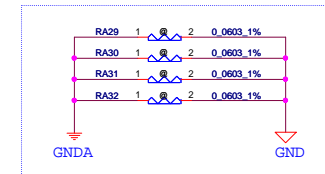
Reserve for cancel issue



JACK_PLUG Delay circuitis



Reserve for cancel Delay circuitis

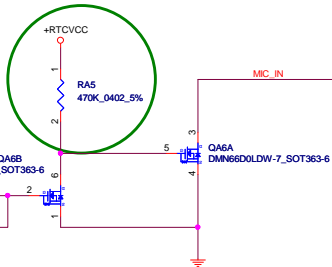


Place on the moat between GND & GNDA.

Latitude Oak Modified

SM01000BV00
need CIS symbol

Latitude Oak Modified

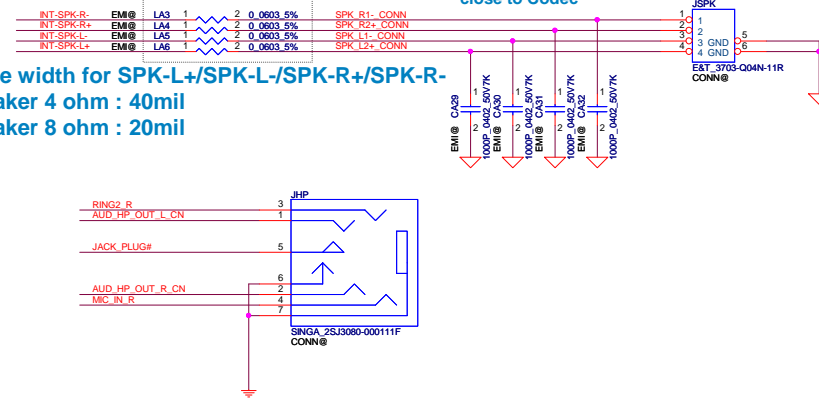
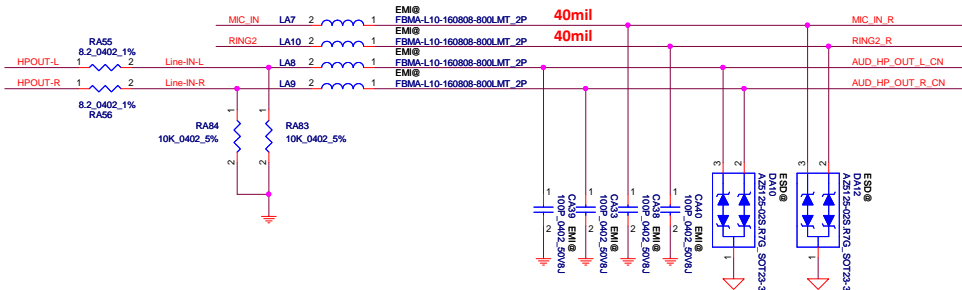


Close to UA1
Pin11,13,14,16

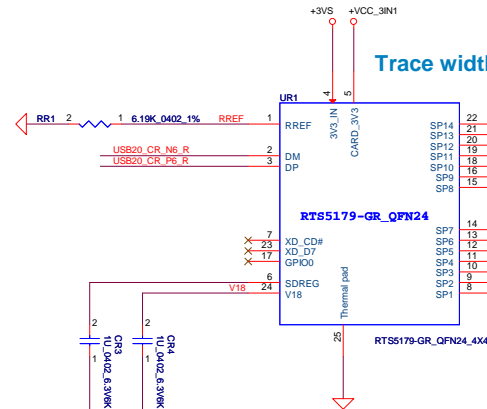
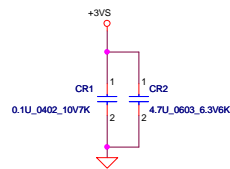
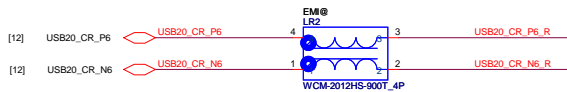
close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

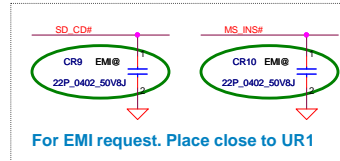
iPhone and Nokia type Combo Jack



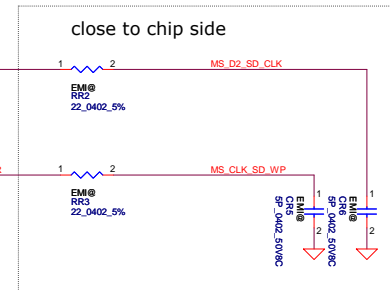
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					0.3
Date:		Thursday, May 23, 2013		Sheet	23 of 58



Latitude Oak Modified



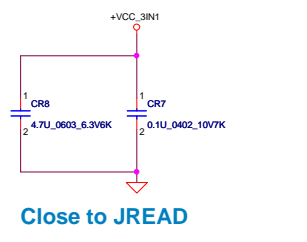
close to chip side



拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

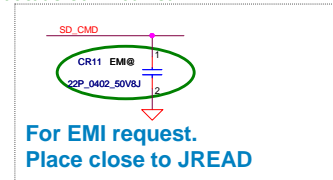
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

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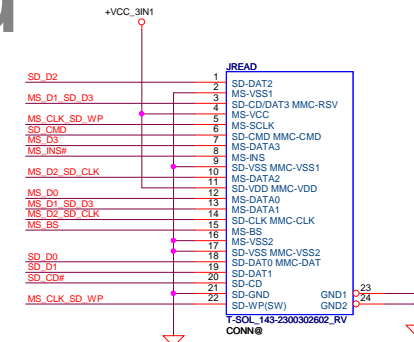


Close to JREAD

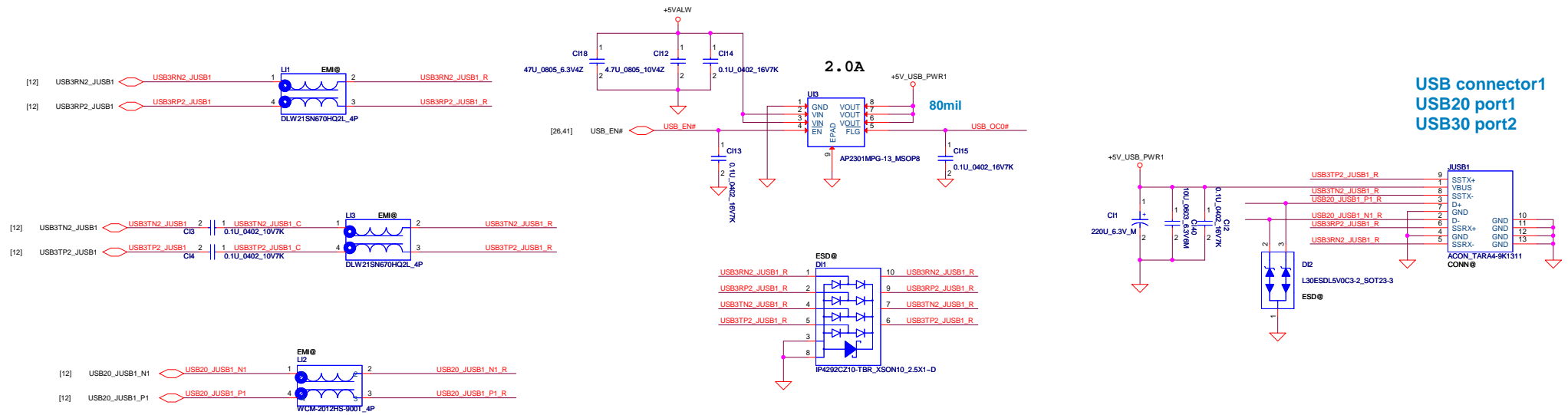
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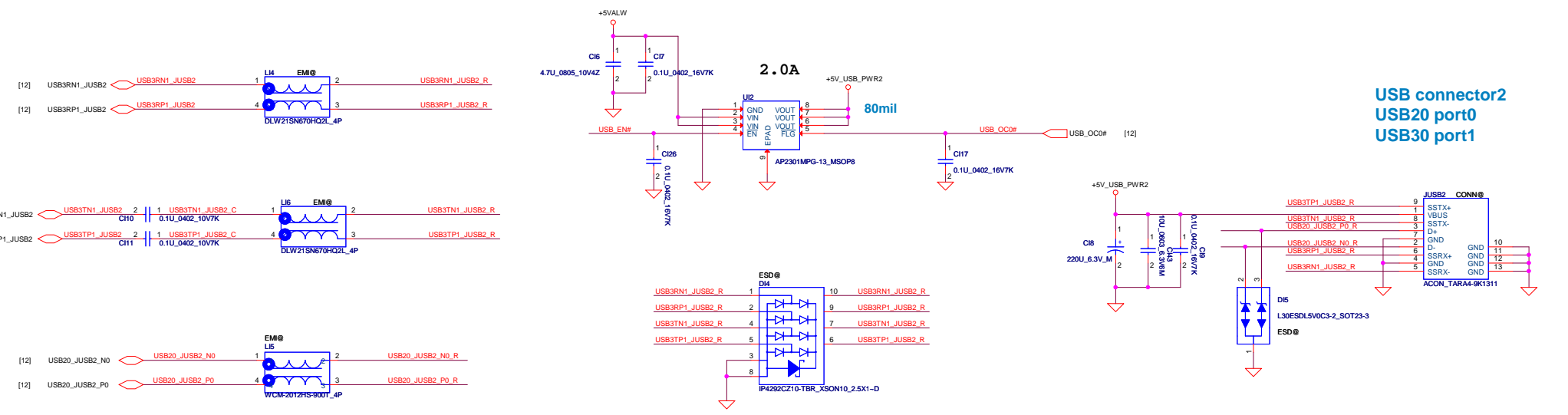
For EMI request.
Place close to JREAD



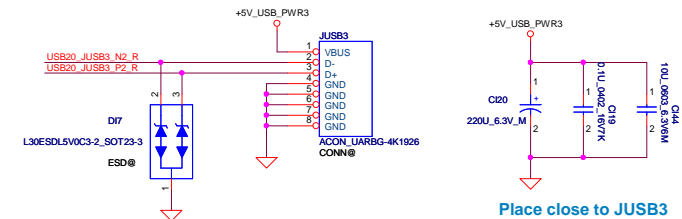
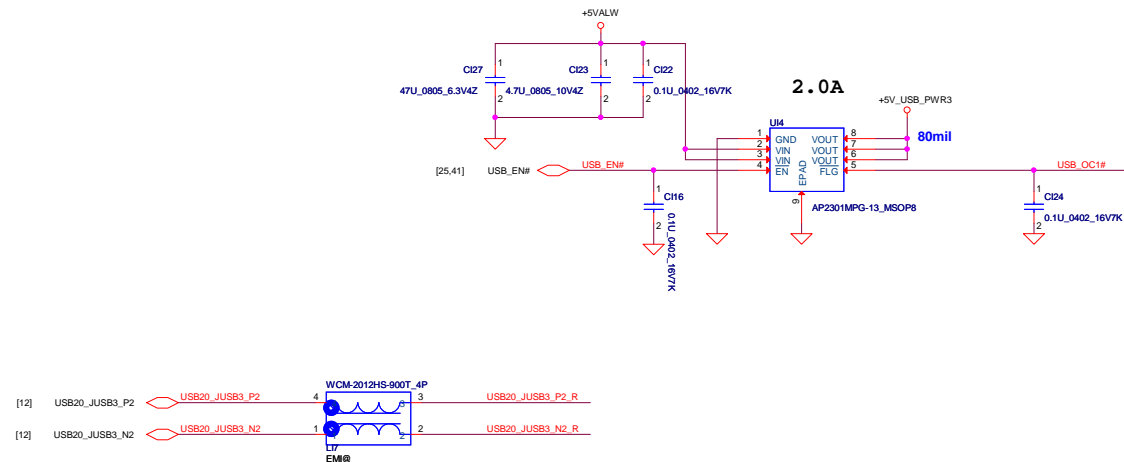
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				Date	Thursday, May 23, 2013
				Sheet	24 of 58
				Rev	0.3



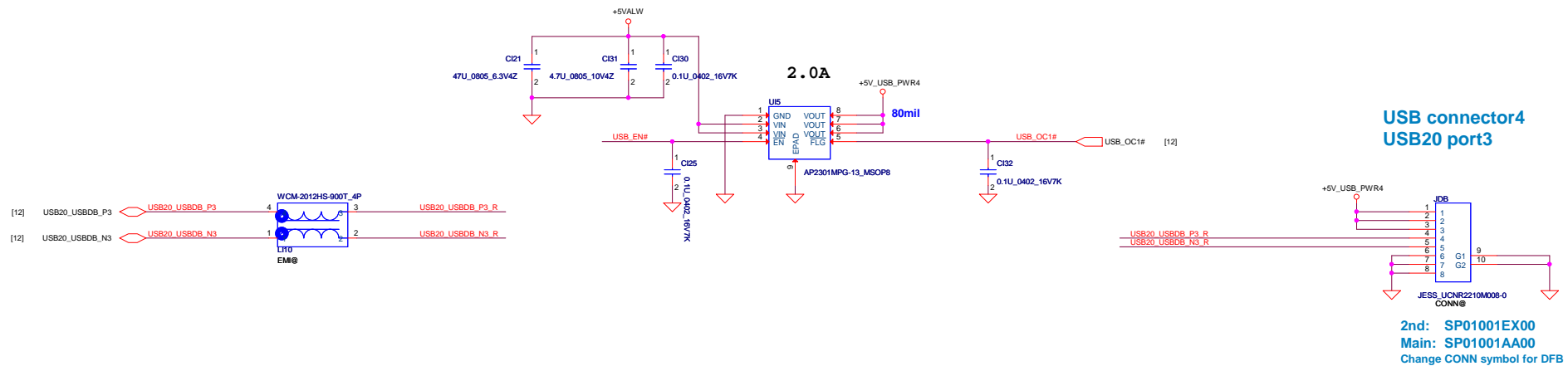
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				Sheet 25 of 58	

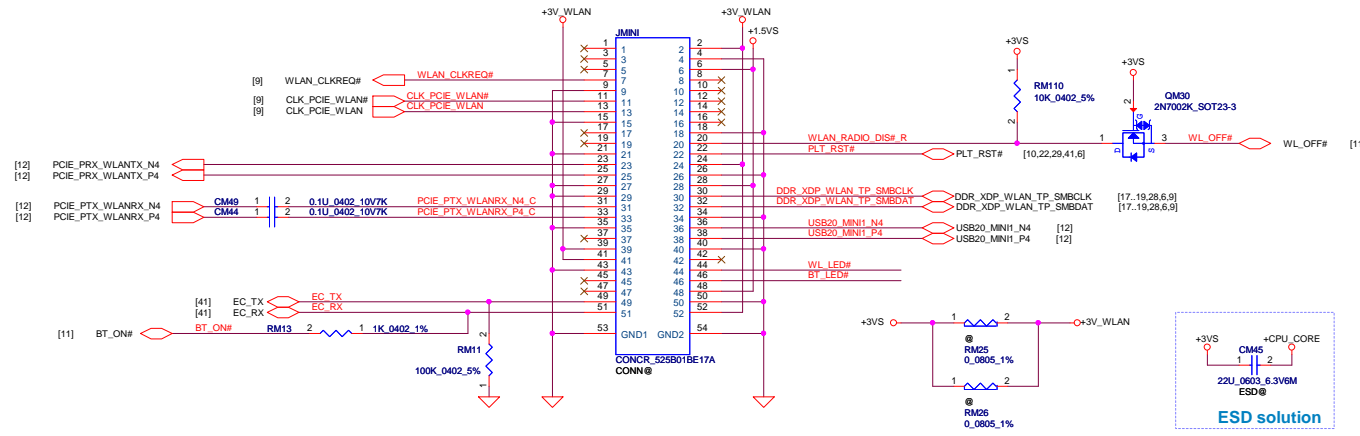


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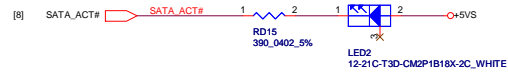


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Mini WLAN/WIMAX H=6.7



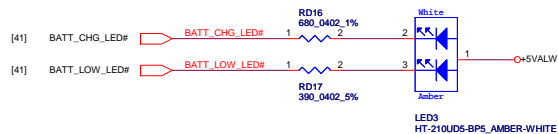
HDD LED



Power LED

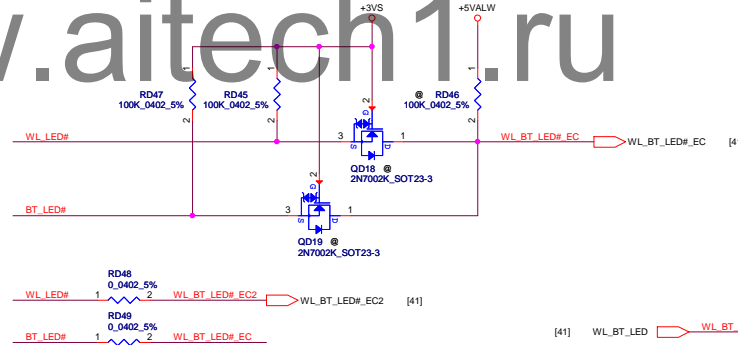


Battery LED

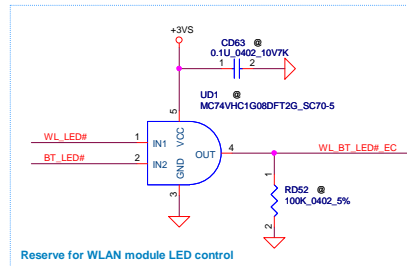
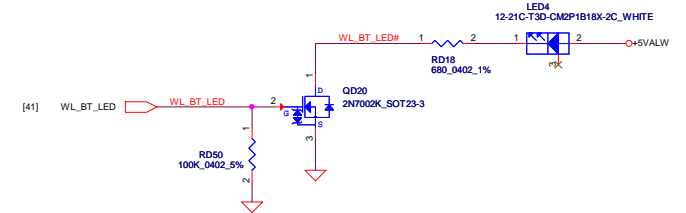


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10mils, All pins



Wireless LED

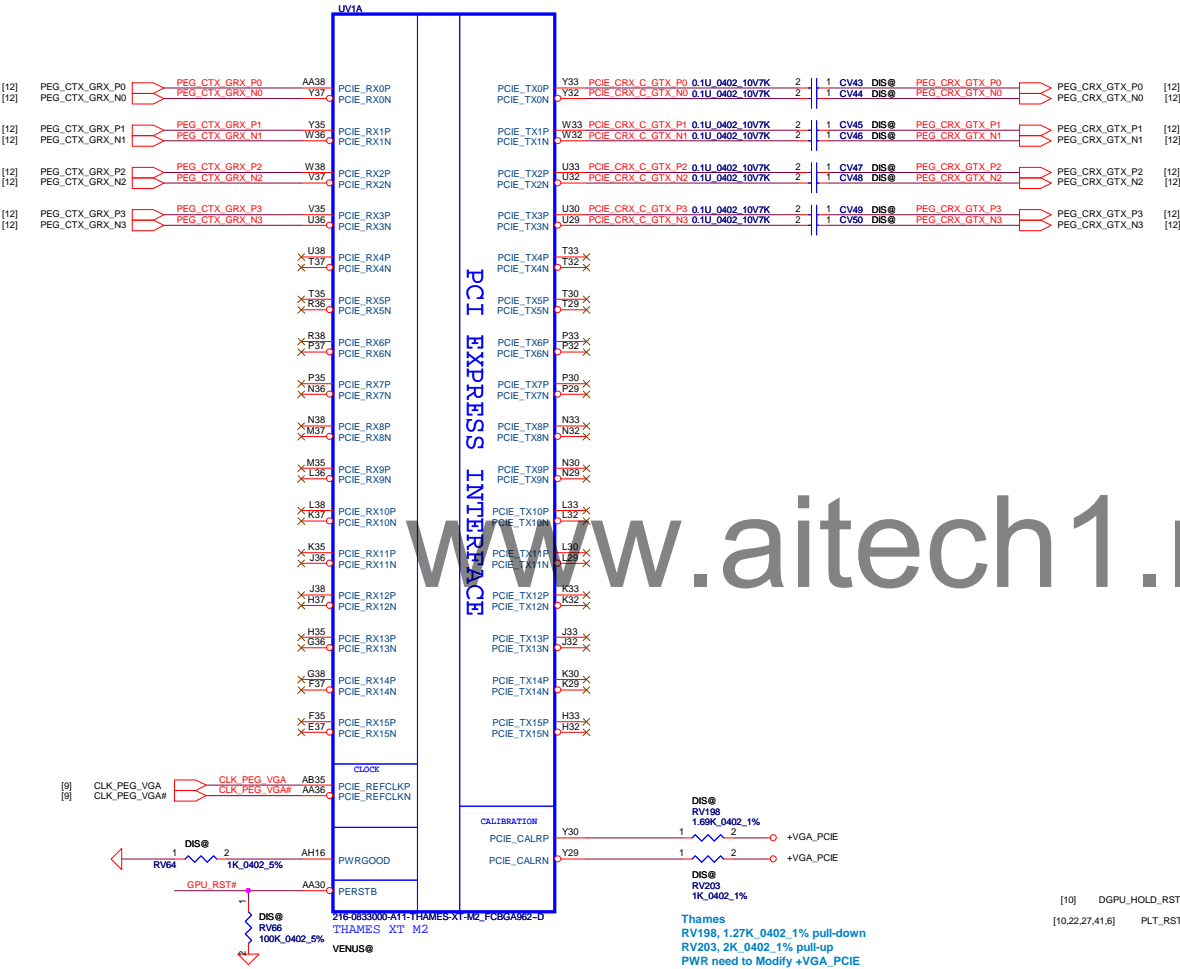


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				Date	Thursday, May 23, 2013
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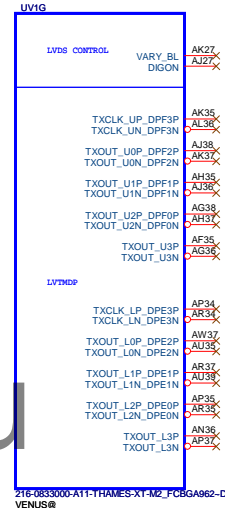


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Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	FAN/TP/PWR SW	
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					LA-A491P	0.3
Date:				Thursday, May 23, 2013	Sheet	26 of 58

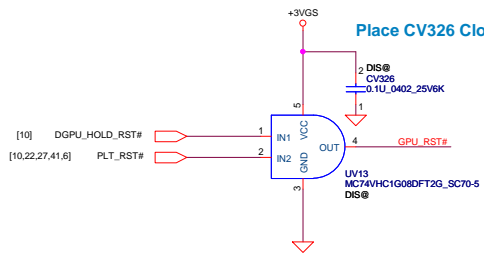
GFX PCIE LANE REVERSAL

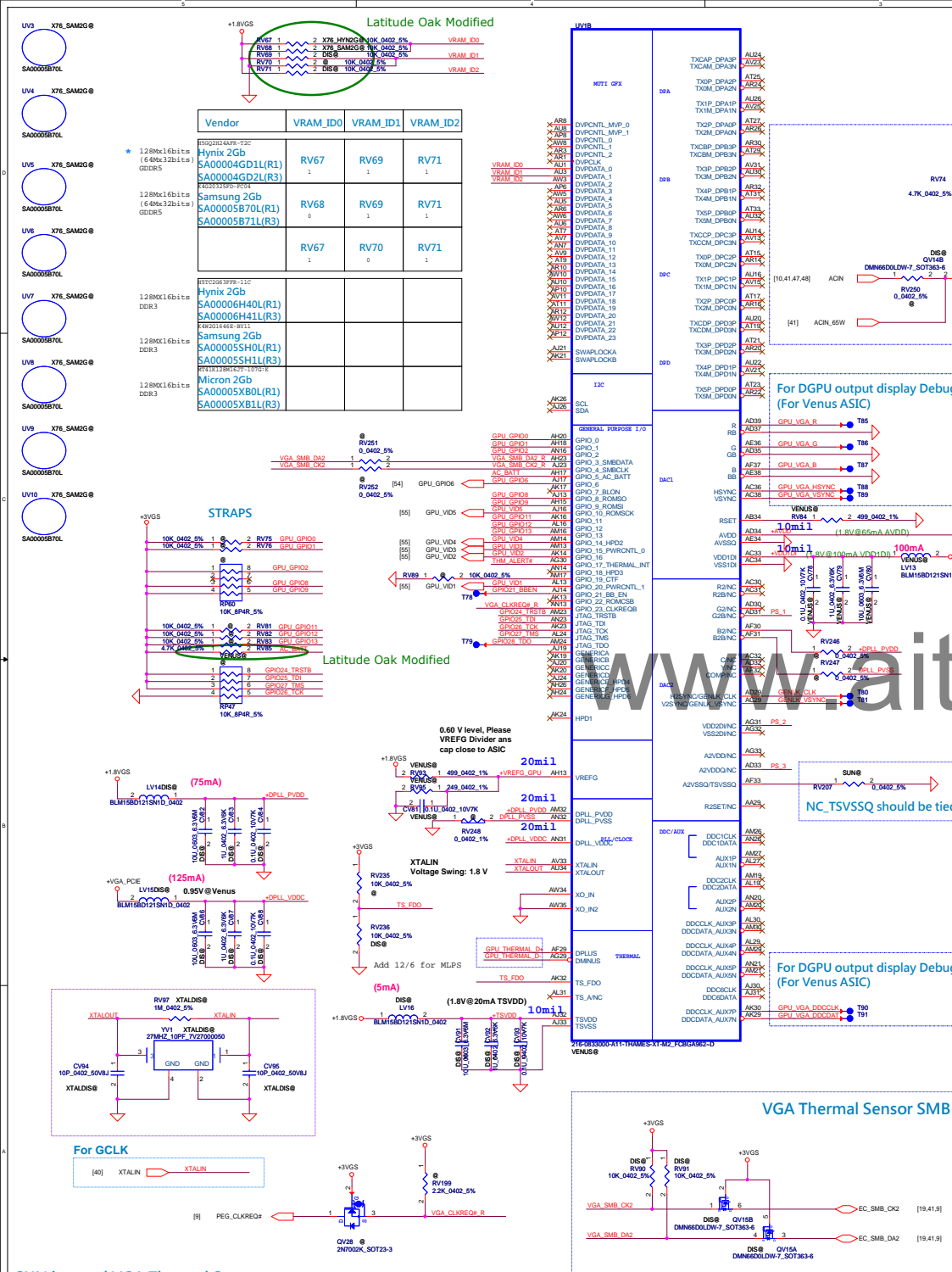


LVDS Interface



Place CV326 Close to UV13





CONFIGURATION STRAPS

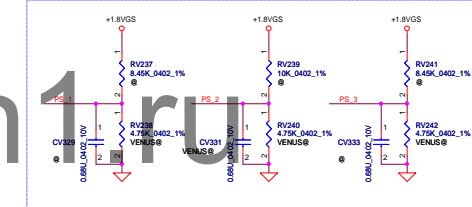
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPIO FULL TX OUTPUT SWING	0: 50% swing 1: full swing
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS	0: disable 1: enable
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.5GT/s 1: 5GT/s
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable
ROMDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VP_DEVICE_STRAP_BNA	V25VNC	IGNORE VIP DEVICE STRAPS	0
RSVD	HS2VNC		0
RSVD	GENERICC		0
ALD[1]	HSYNC	ALD[1] ALD[0] 0: No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	11
ALD[0]	VS2VNC		0

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	HSYNC	GENERICC	GPIO2	GPIO8
--------	-------	----------	-------	-------

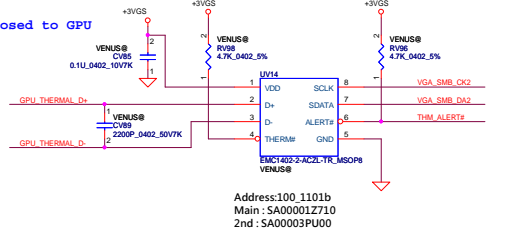
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



SUN MLPs PS_3	RV241	RV242	Bits [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

VENUS MLPs PS_3 used default

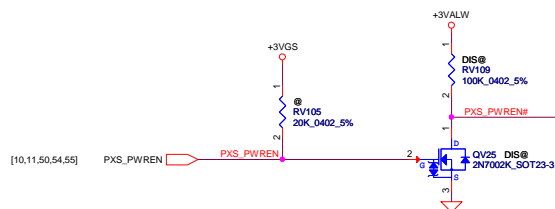
External Thermal Sensor EMC1402-2-ACZL-TR



PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3,PCIE_VDDC and 1.8V rail

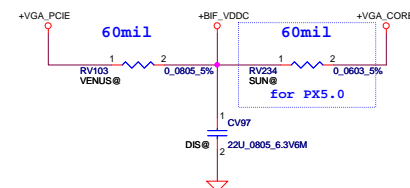
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF



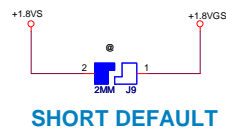
for PX4.0 and PX5.0

Switch circuits in BACO desings for Thames/Seymour only
55mA@1.0V, in BACO mode

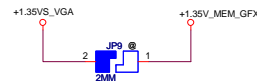


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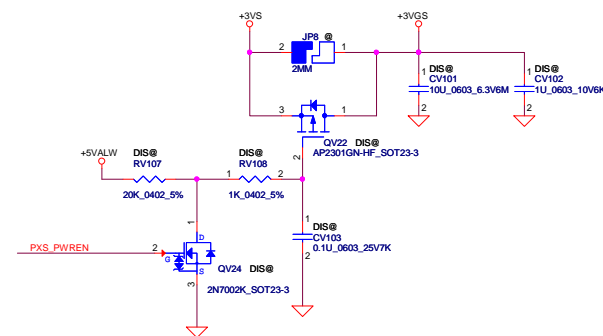
+1.8VS TO +1.8VGS



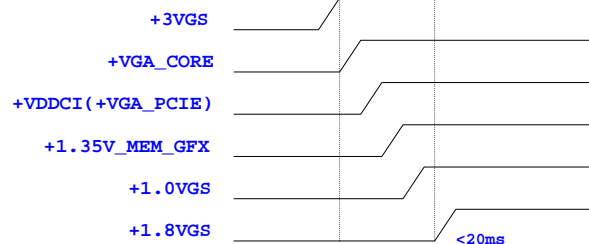
+1.35VS_VGA TO +1.35V_MEM_GFX



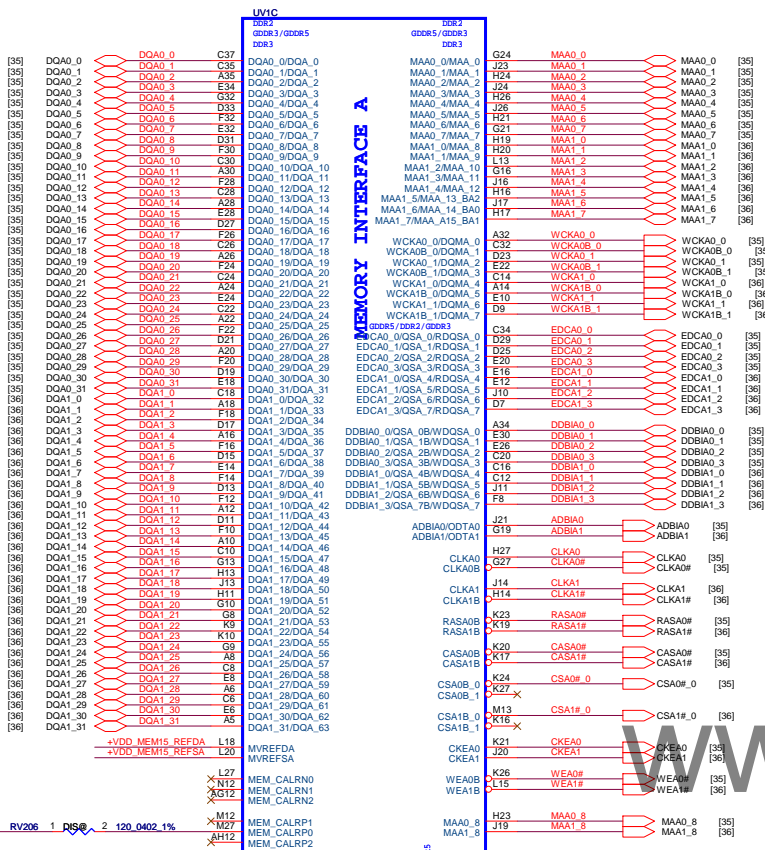
+3VS TO +3VGS



Power sequence of Sun XT,Venus Pro,Venus XT

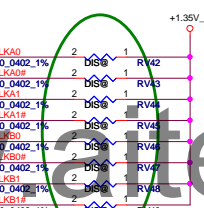


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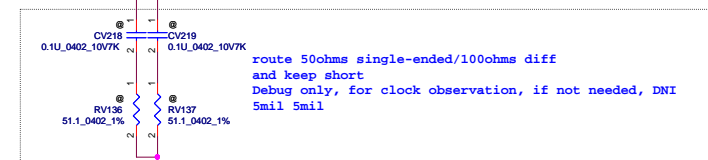
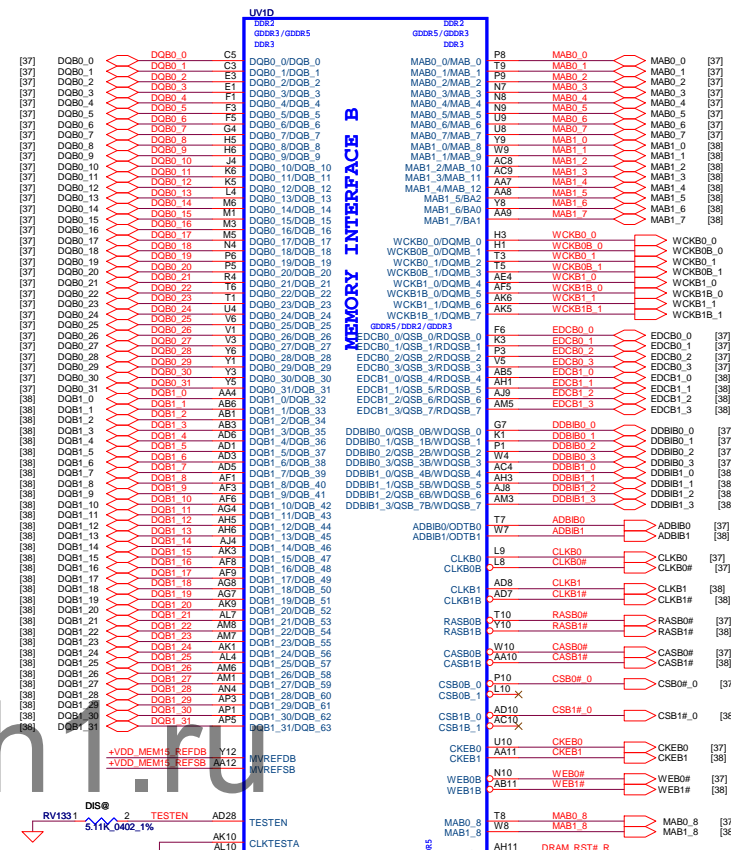


GDDR5 CMD Mapping Table

	<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#	
CMD15	CMD31	CAS#	
CMD5	CMD21	WE#	
CMD0	CMD16	CS#	
CMD8	CMD24	ABIT#	
CMD10	CMD26	A0_A10	
CMD17	CMD27	A1_A9	
CMD18	CMD18	A2_BA0	
CMD1	CMD17	A3_BA3	
CMD3	CMD15	A4_BA2	
CMD4	CMD20	A5_BA1	
CMD7	CMD23	A6_A11	
CMD9	CMD22	A7_A10	
CMD14	CMD25	A12_FRU	
CMD13	CMD30	CKE#	
	CMD29	RESET#	

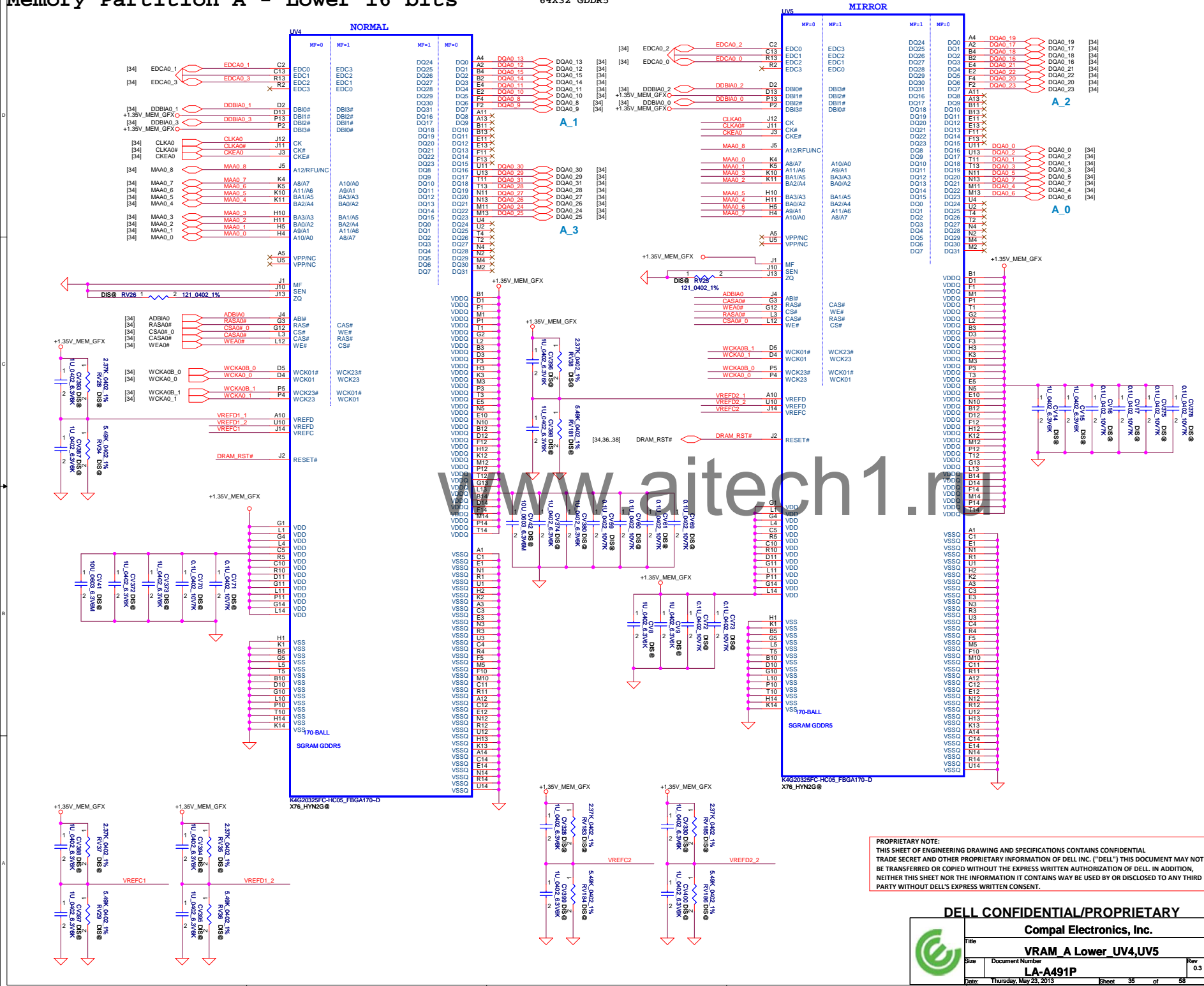


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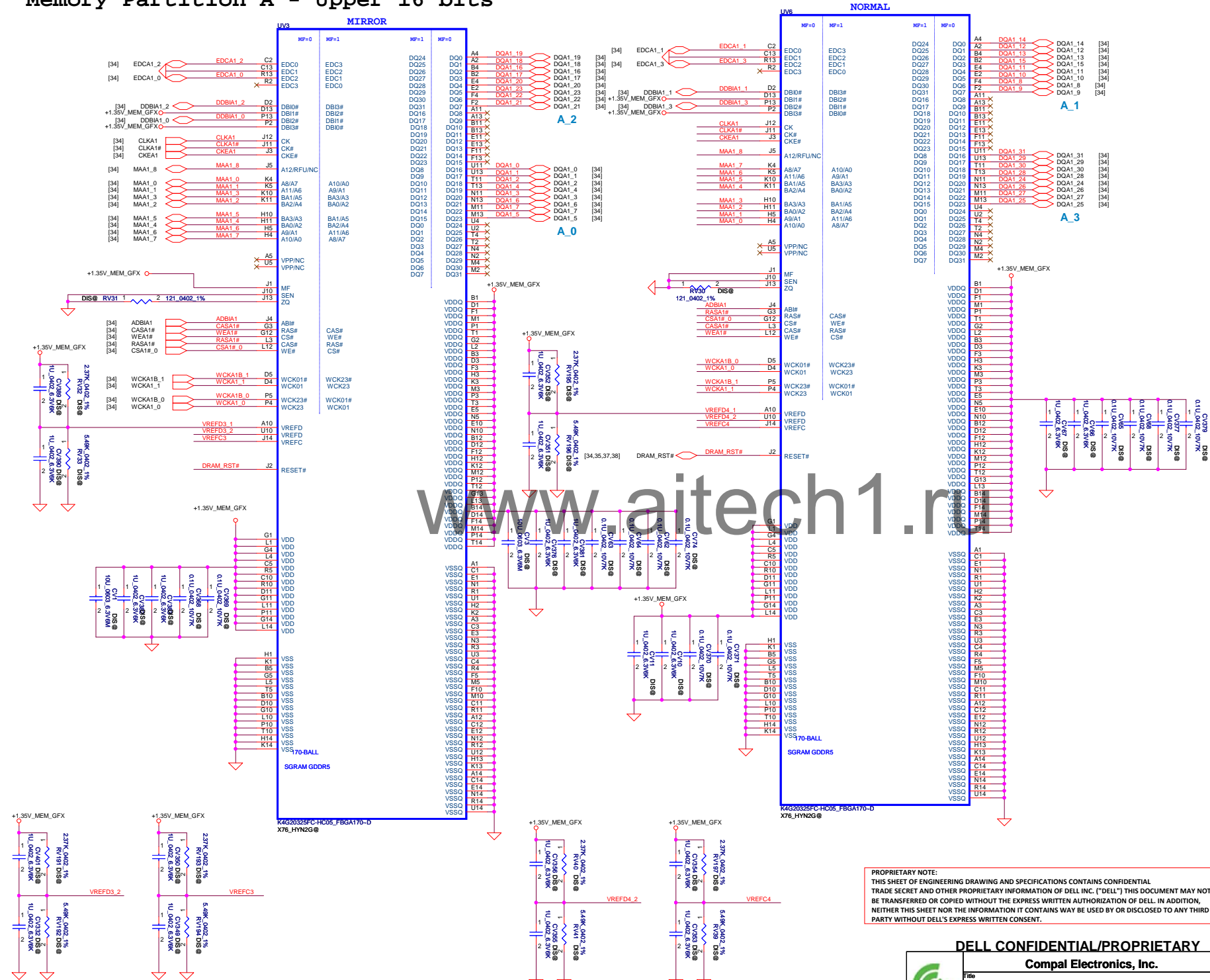
Memory Partition A - Lower 16 bits

64X32 GDDR5



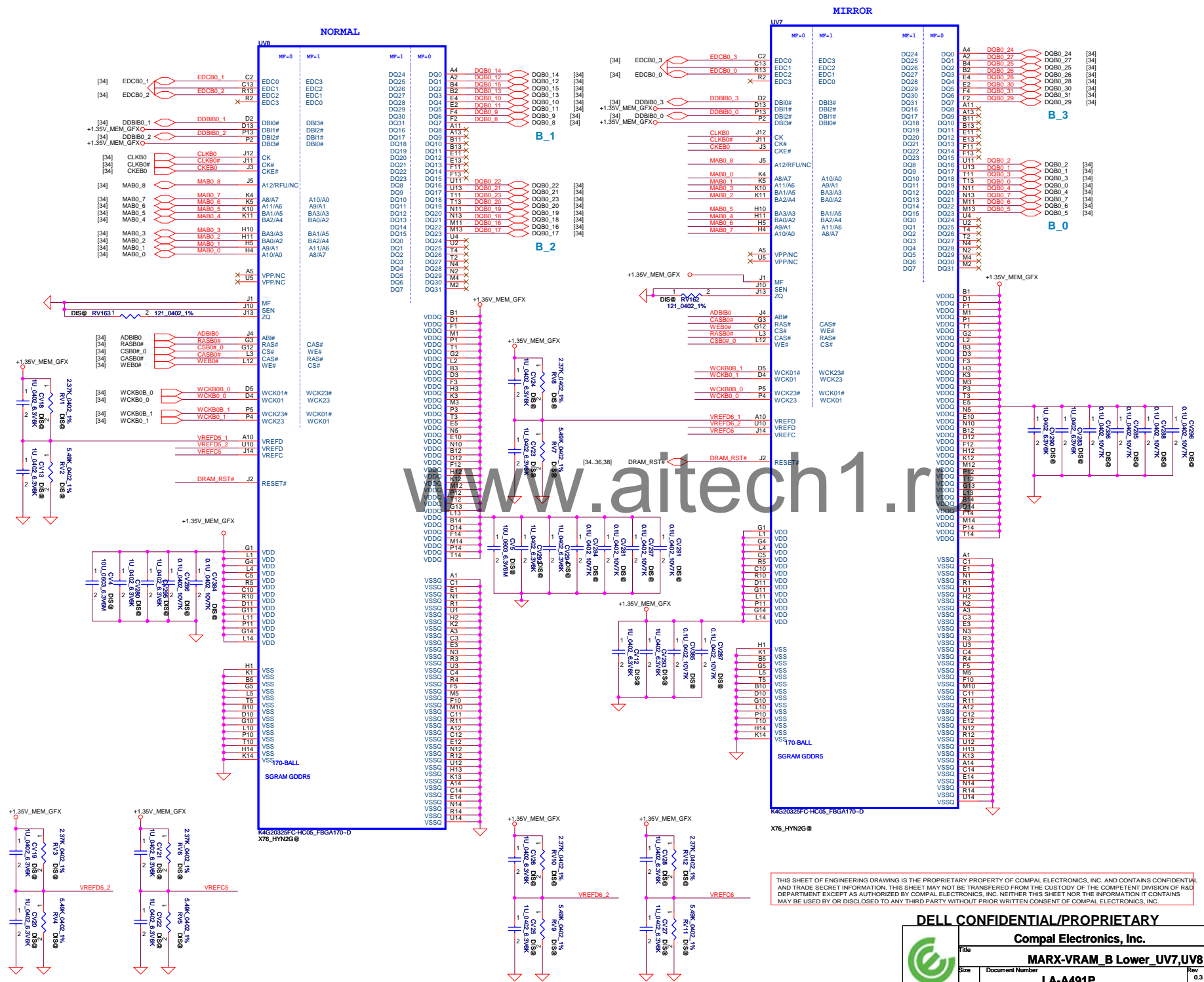
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Memory Partition A - Upper 16 bits



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Memory Partition B - Lower 16 bits



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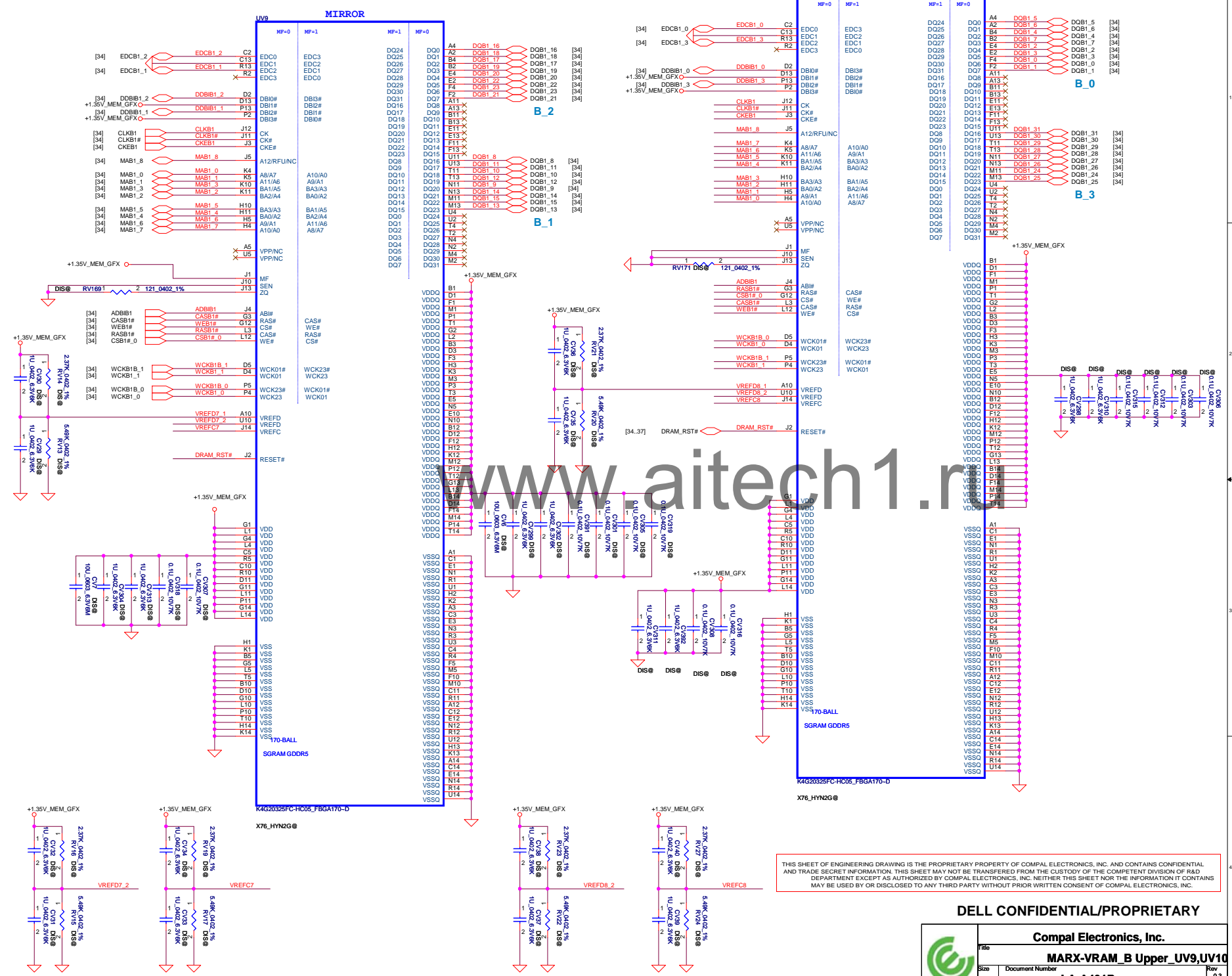
MARX-VRAM_B Lower UV7,UV8

LA-A491P

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Memory Partition B - Upper 16 bits

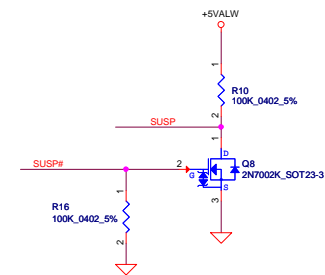
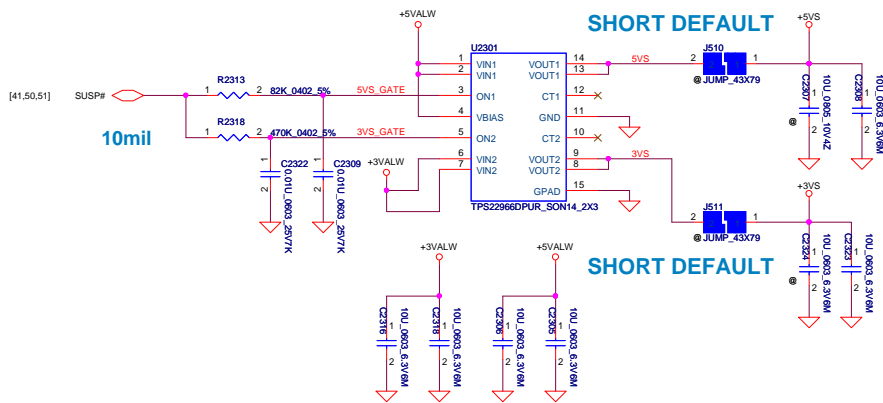


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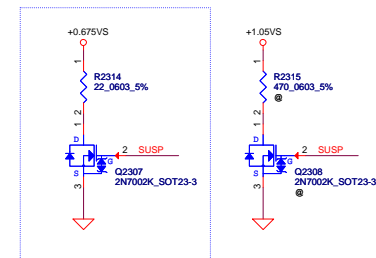
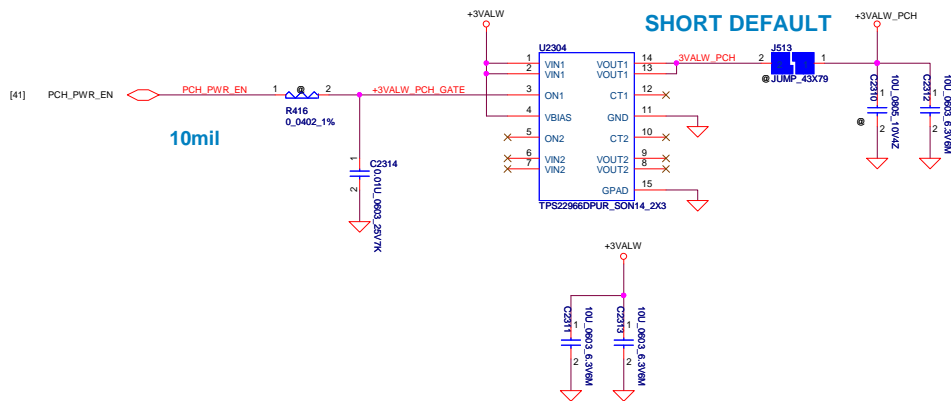
		Compal Electronics, Inc.	
File	Document Number	MARX-VRAM_B_Upper_UV9,UV10	
Size	Rev	LA-A491P	
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+5VS and +3VS switch



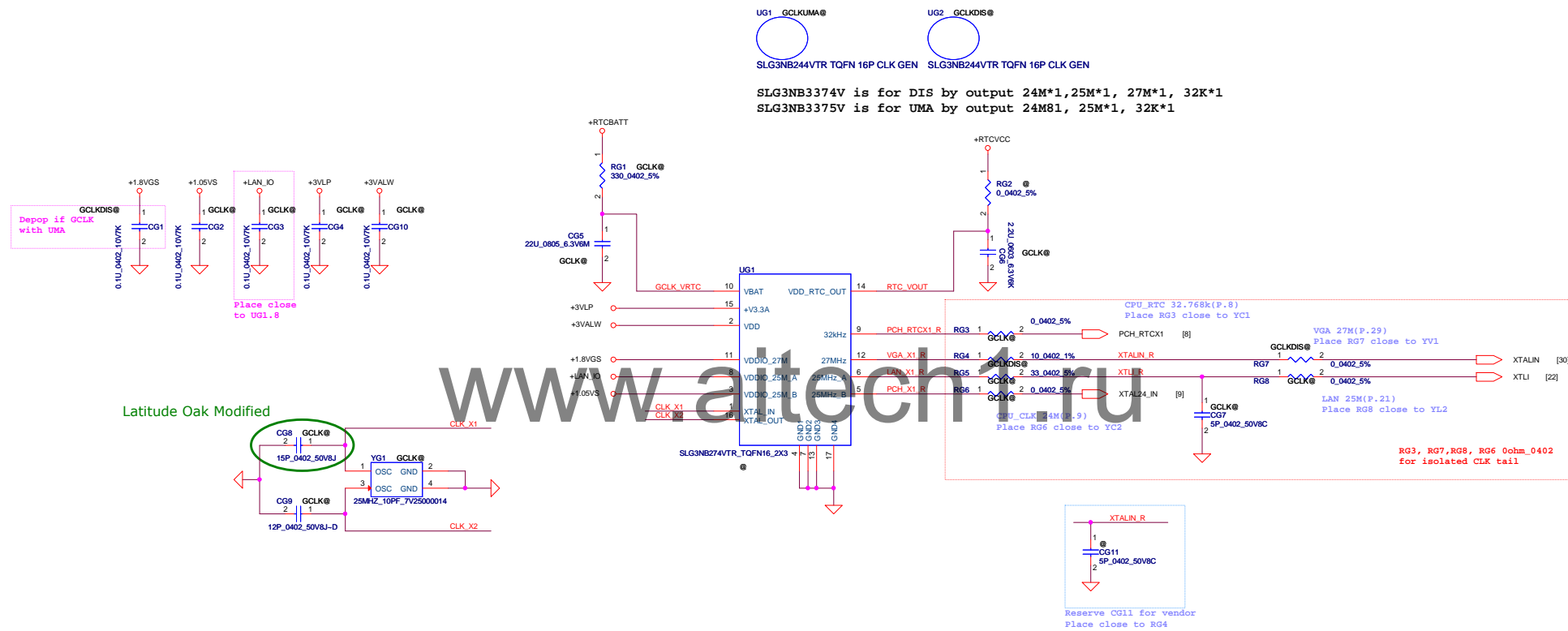
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+3VALW_PCH switch

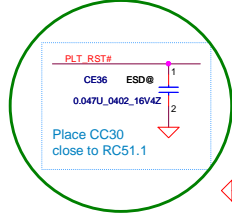


For Intel S3 Power Reduction

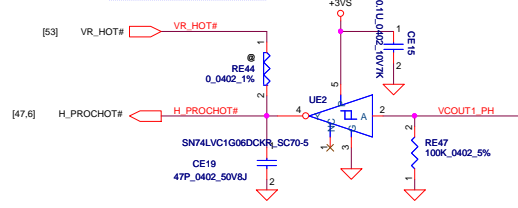
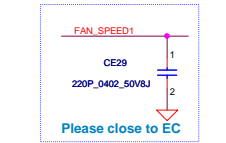
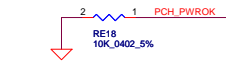
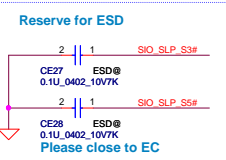
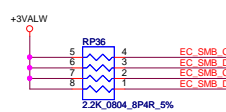
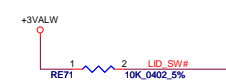
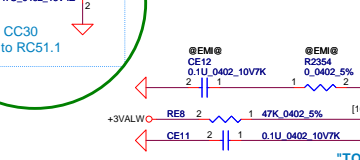
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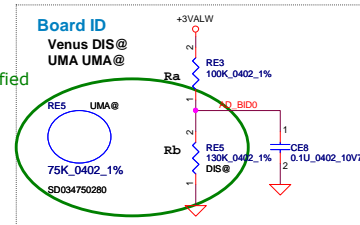


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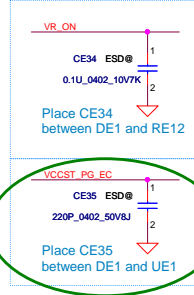


KB9012A3 change to
KB9012A4 SA00004OB30

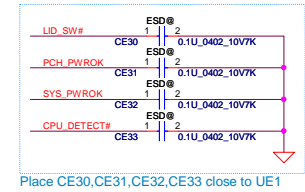
Latitude Oak Modified



Latitude Oak Modified

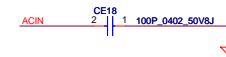


Latitude Oak Modified



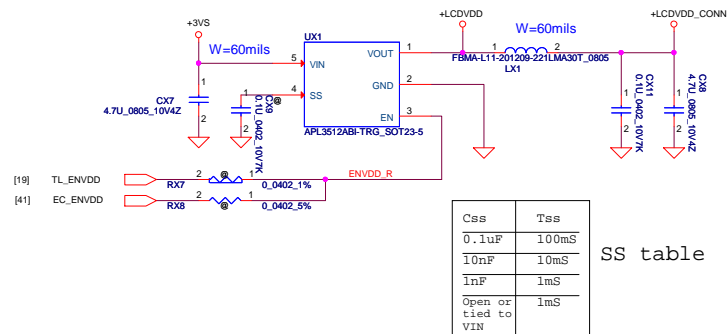
Place CE30, CE31, CE32, CE33 close to UE1

ME_FWP PCH has internal 20K PD.
(suspend power rail)

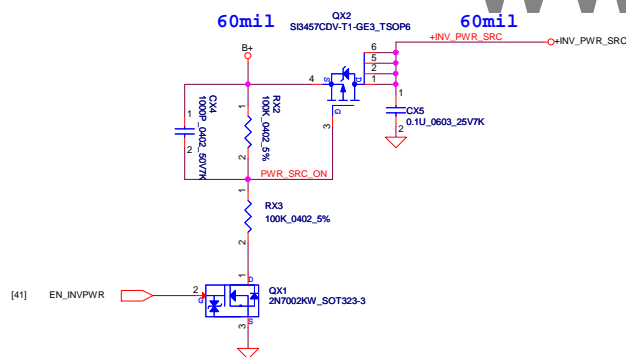


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Issued Date		Deciphered Date		EC ENE-KB9012	
2013/03/06		2014/04/01		Document Number	
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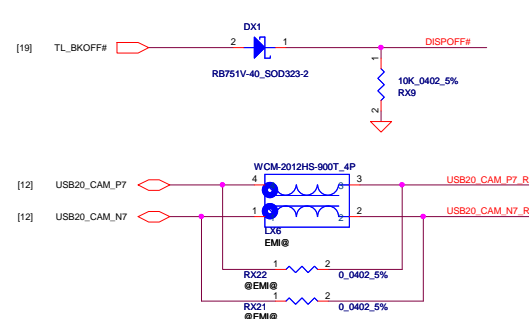
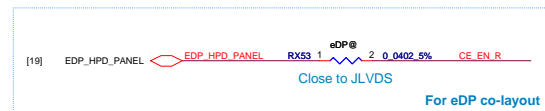
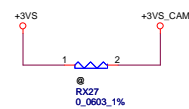
LCD PWR CTRL



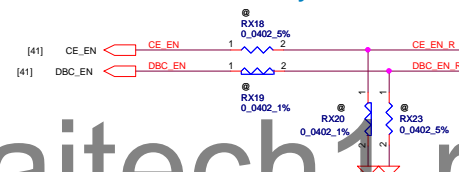
LCD backlight PWR CTRL



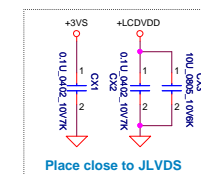
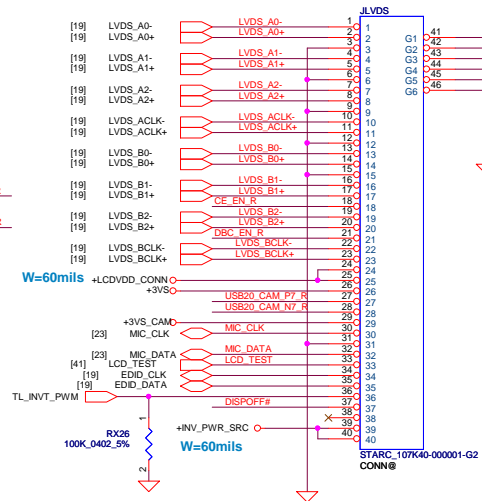
Webcam PWR CTRL



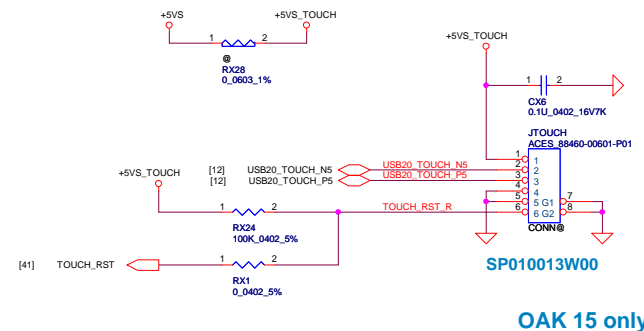
CE_EN_R only for reserve.



LVDS Connector

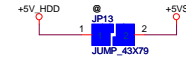


*** Touch Screen Panel**

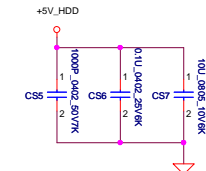
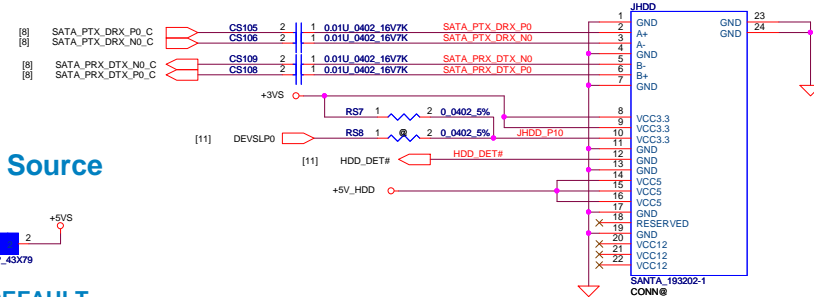


SATA HDD Connector

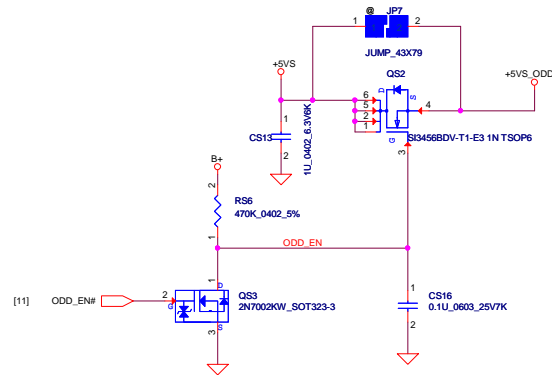
+5V_HDD Source



SHORT DEFAULT

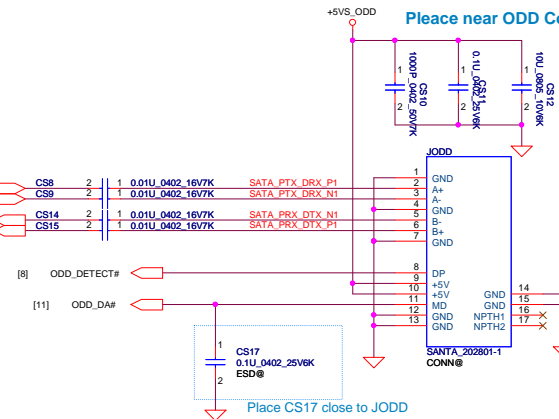


ODD Power Control



SATA ODD Connector

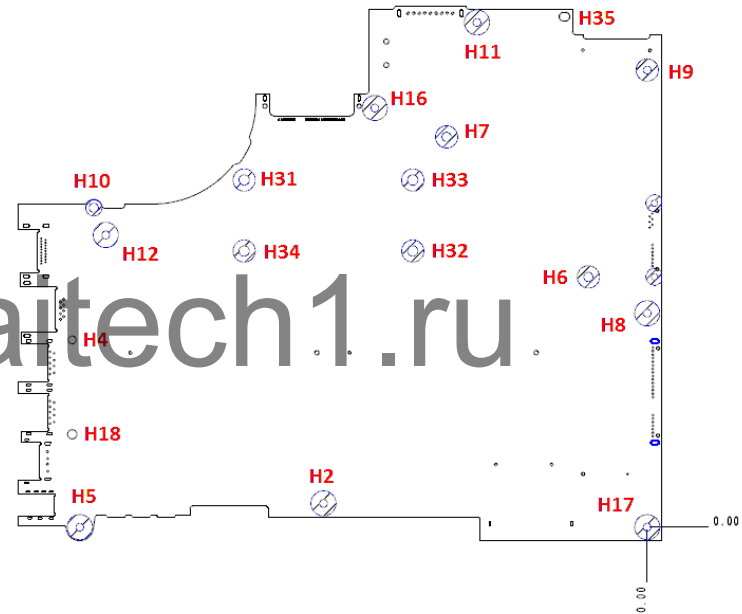
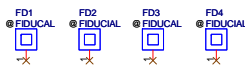
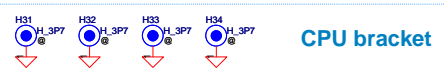
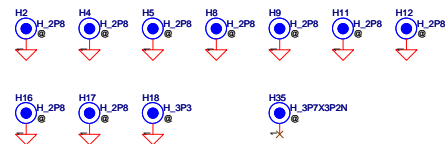
Place near ODD Connector



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Screw Hole



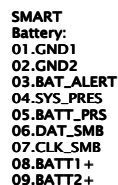
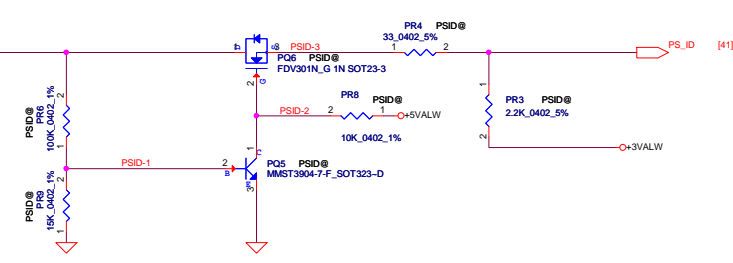
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Issued Date	2013/03/06	Deciphered Date	2014/04/01	Title	Screw Hole
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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ADP_I (with selector)

VCIN1_PH

PR23 150K_0402_1%

PR26 499K_0402_1%

PC13 1U_0402_16V7K

PC14 1U_0402_16V7K

P04 2N7002W-T1/R7_SOT323-3

65W/90V

Delay adaptor OC_H_PROCHOT#

2ms while hybrid power transition

VCOUT1_PH

PR30 160K_0402_1%

PC15 0.01U_0402_25V7K

P03A L2N7002DWTTG_S08B-6

H_PROCHOT#

PH1 under CPU bottom side

CPU thermal protection at 93 +/- 3 degree C

REC_VCCA

VCIN0_PH

PR24 12.1K_0402_1%

PC16 100K_0402_1%_TSM08104F4251RZ

P01B L2N7002DWTTG_S08B-6

PH1

Adapter protection:

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

BATT_PR51

PR31 1M_0402_1%

PR33 1M_0402_1%

PC14 1U_0402_16V7K

P02B L2N7002DWTTG_S08B-6

H_PROCHOT#

Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

VIN

PR31 1M_0402_1%

PR33 1M_0402_1%

PC16 1U_0402_16V7K

P02B L2N7002DWTTG_S08B-6

H_PROCHOT#

Erp lot6 Circuit

VIN

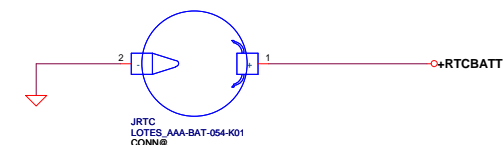
PR7 1M_0402_1%

PR10 1M_0402_1%

PC15 1U_0402_25V

P01A L2N7002DWTTG_S08B-6

H_PROCHOT#

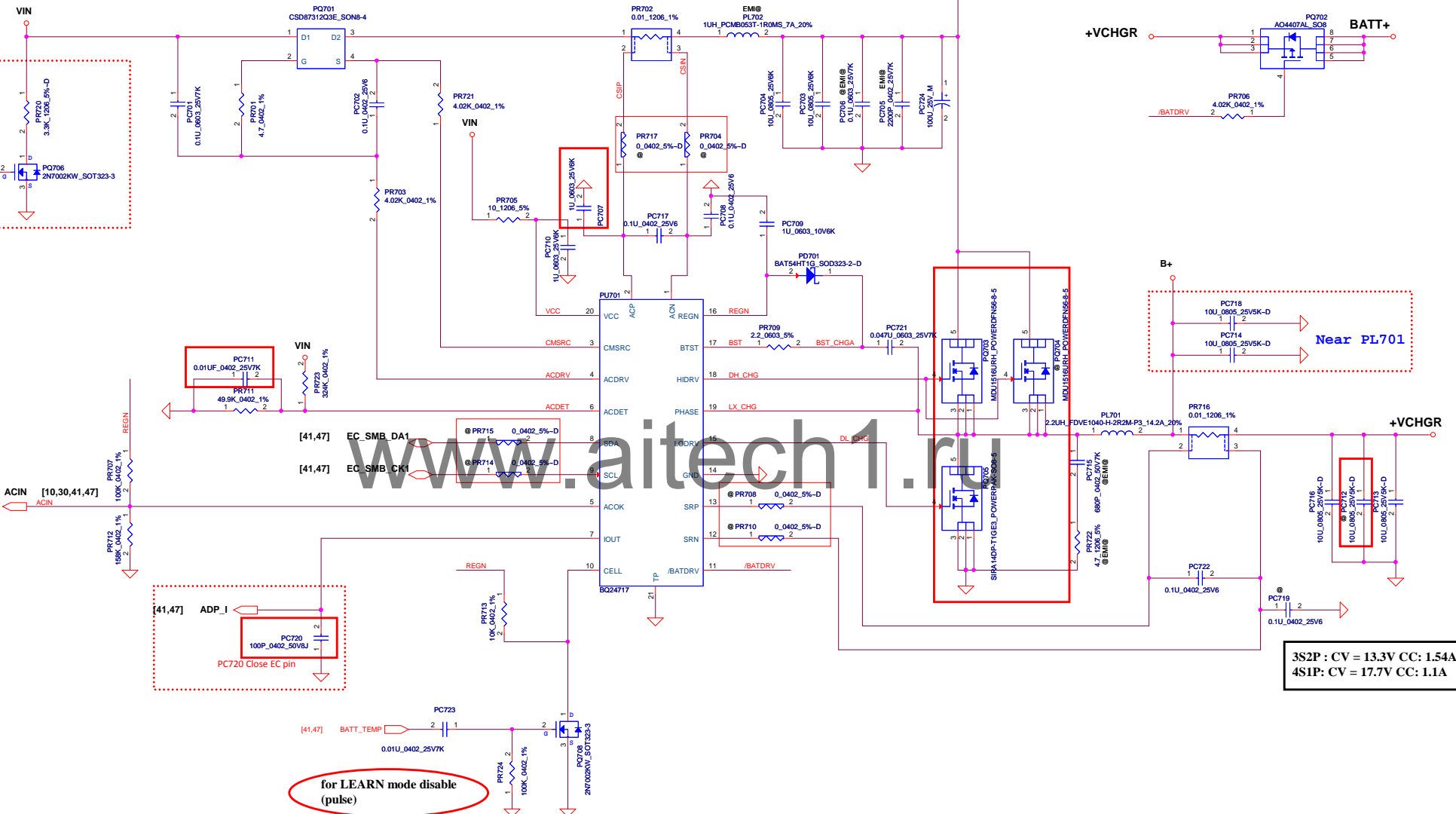


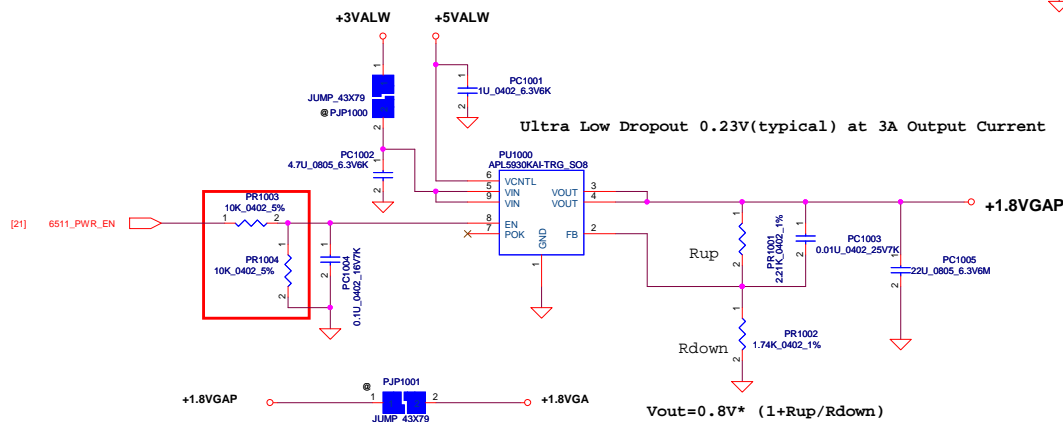
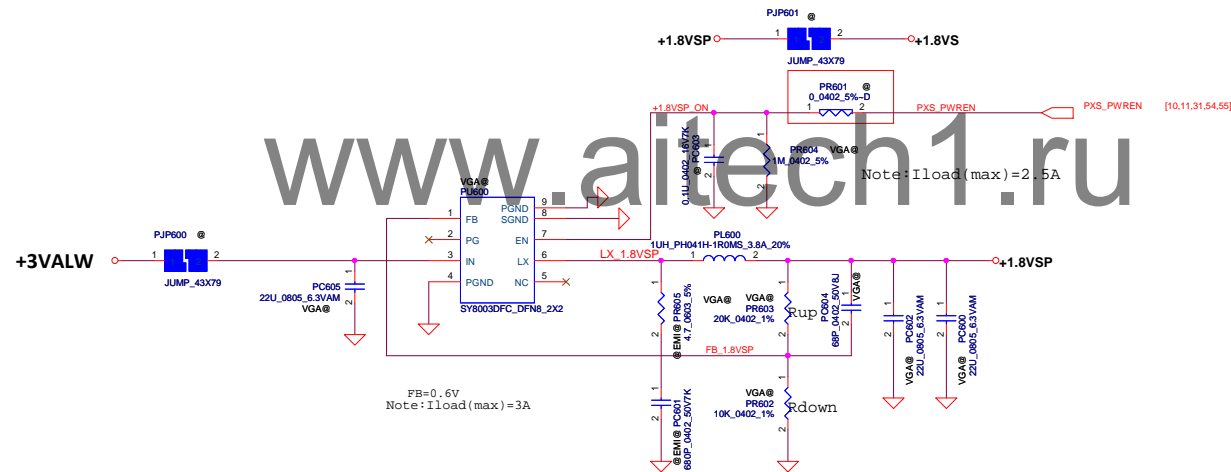
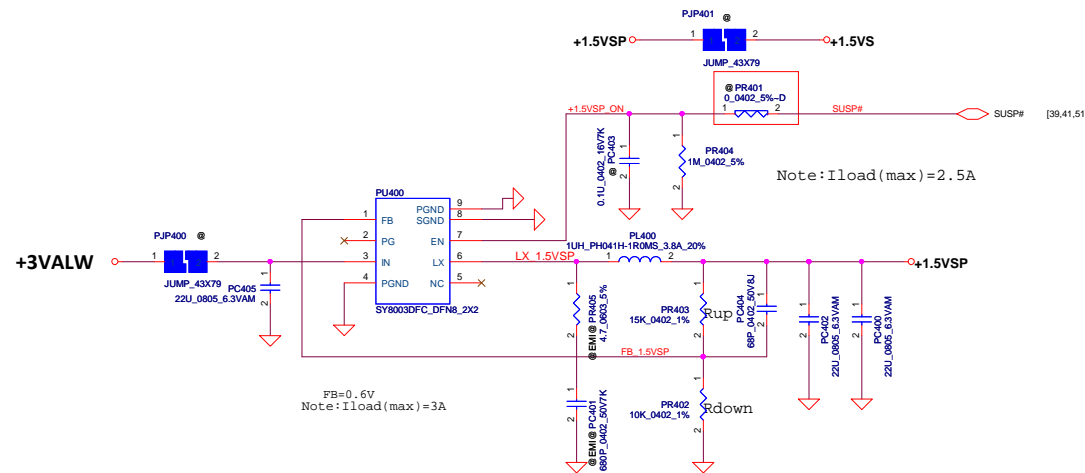
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>	
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Iada=0~3.33A(65W)

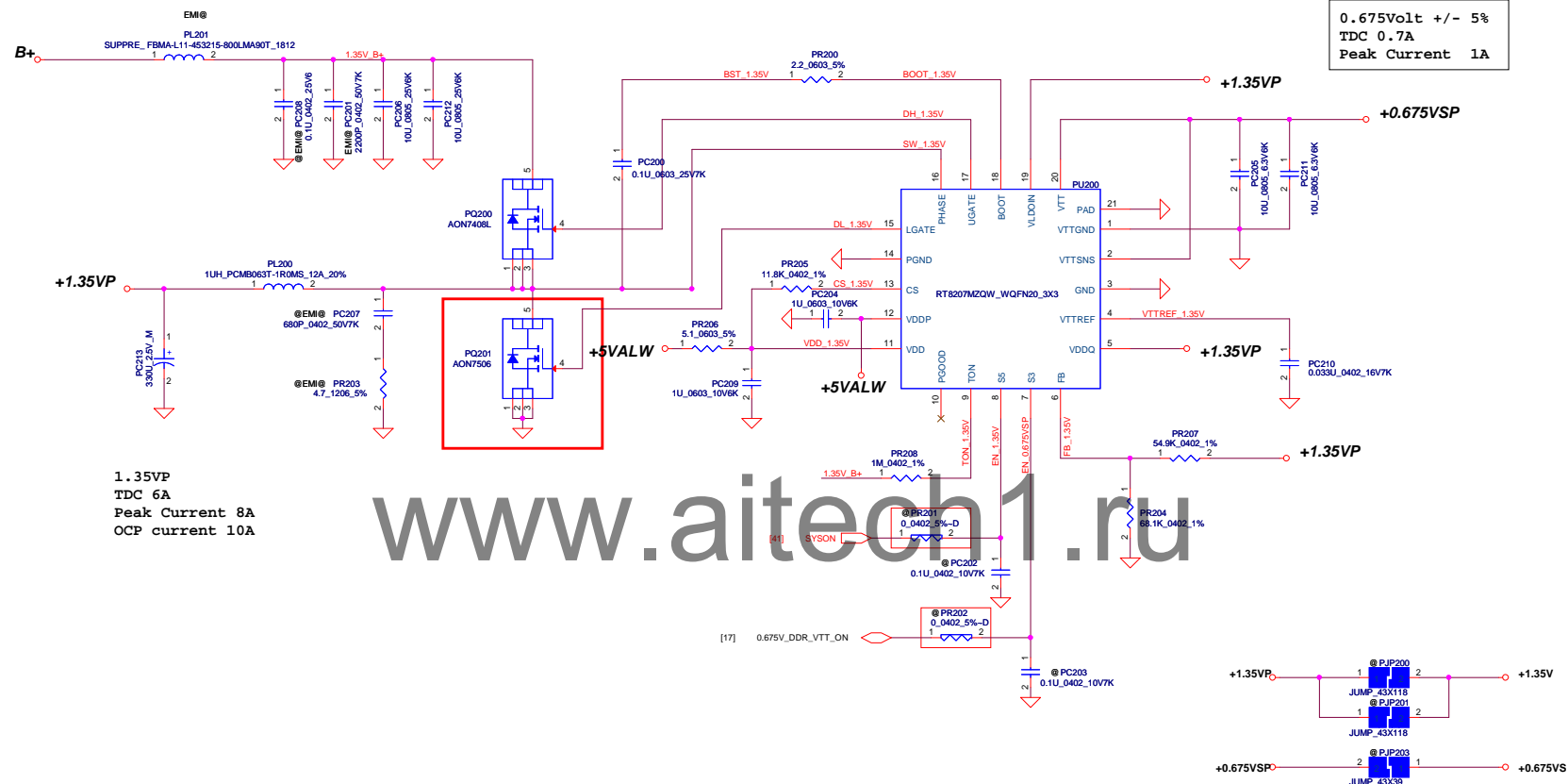
Iada=0~4.62A(90W)

ADP_I = 40*Iadapter*Rsense



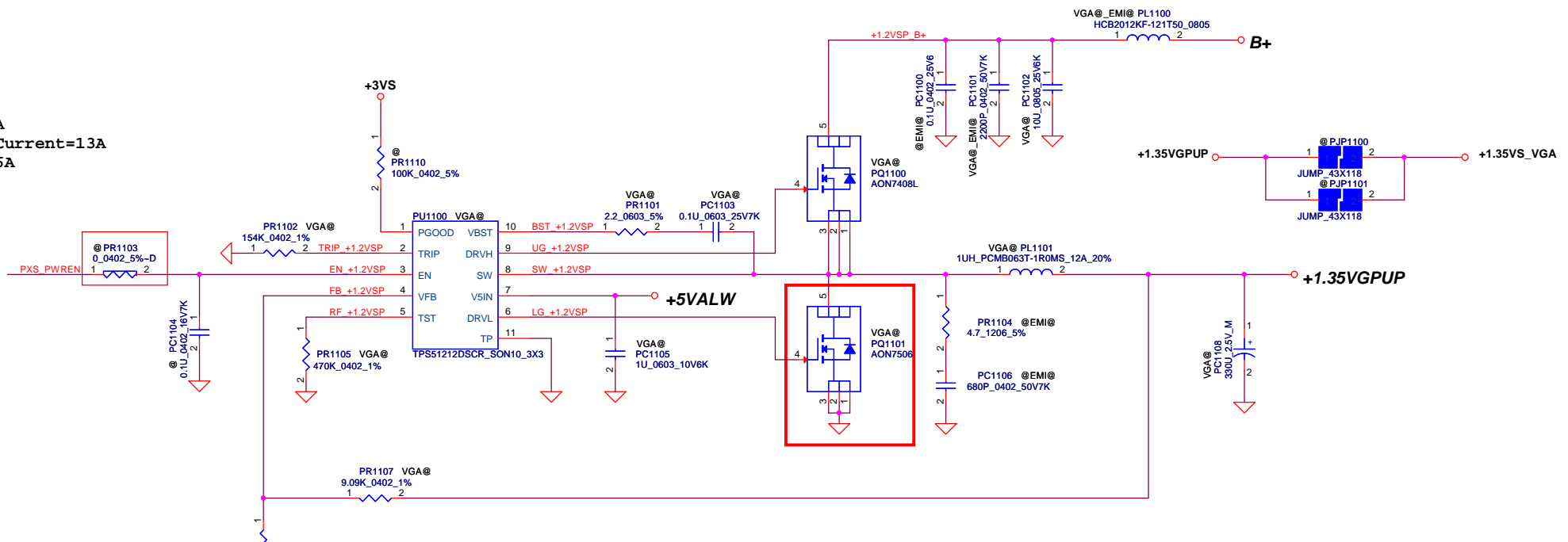


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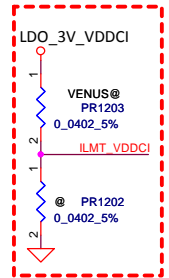
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/03/09	Deciphered Date	2014/04/01	Title	PWR +1.35VP/0.675VSP
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TDC=9A
Peak Current=13A
OCP=16A

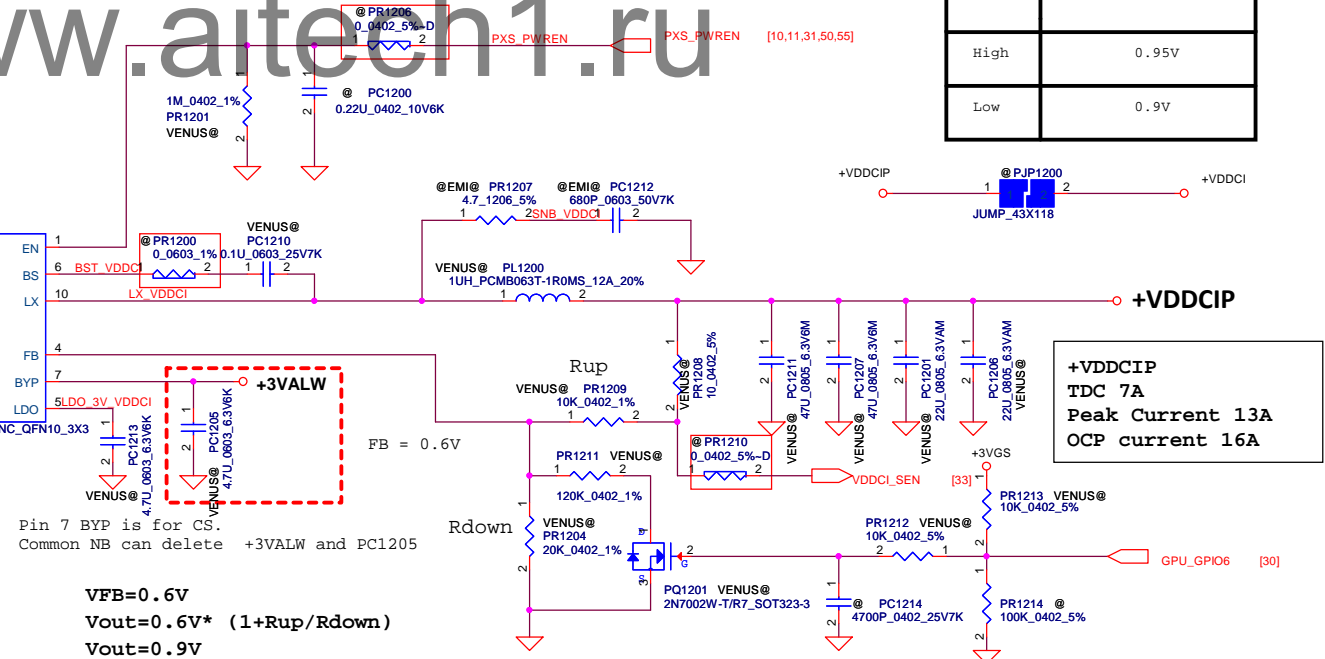


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	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

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	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA CORE

Frequency 300kHz

TDC 23A (25W) / 33A (32W)

Peak Current 30A (25W) / 47A (32W)

OCF current 36A (25W) / 56A (32W)

TYP MAX

H/S Rds(on) : 12.2mohm , 15mohm

L/S Rds(on) : 2.75mohm , 3.5mohm

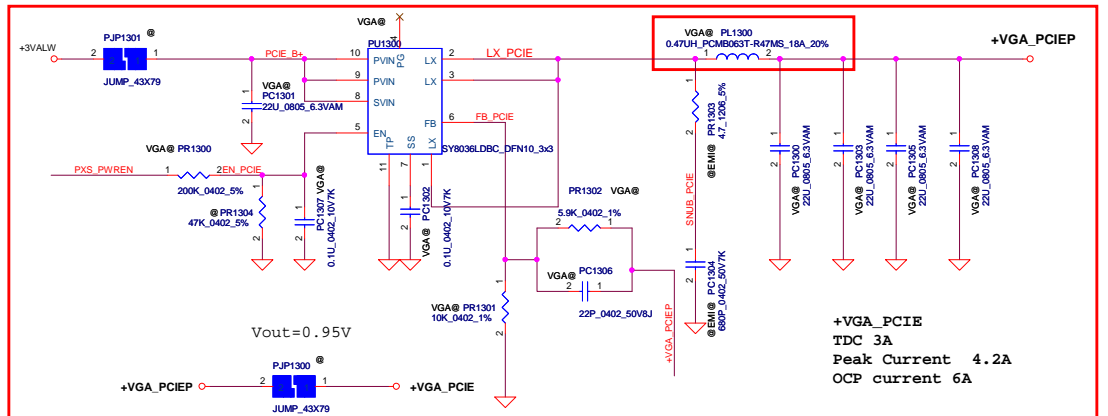
Choke DCR 1.1mohm (Typ) / 1.3mohm (Max)

Load line : -1.5mV/A

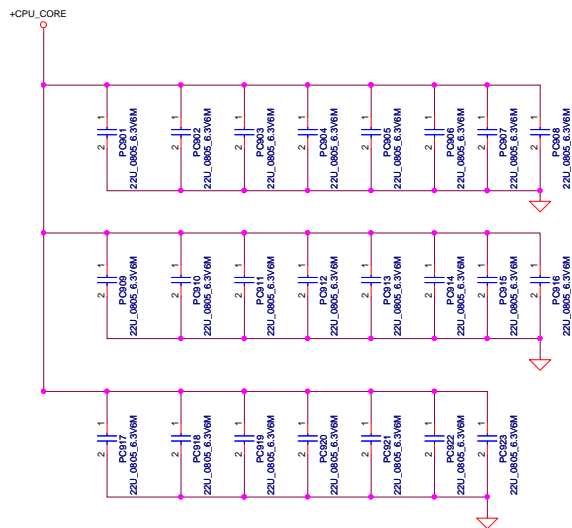


GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

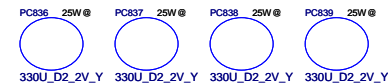
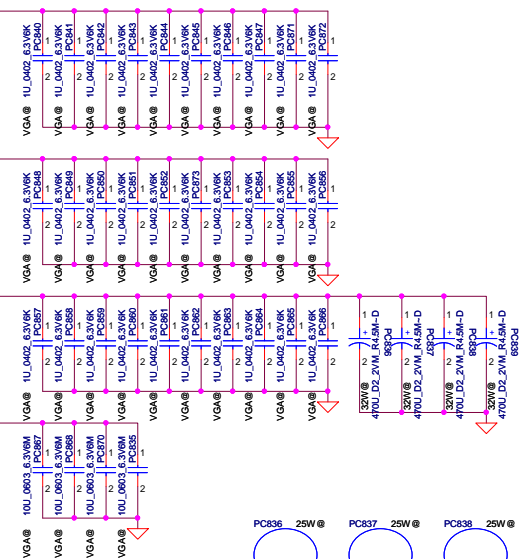
Initial voltage: 0.85V (Venus)
0.9V (Sun)



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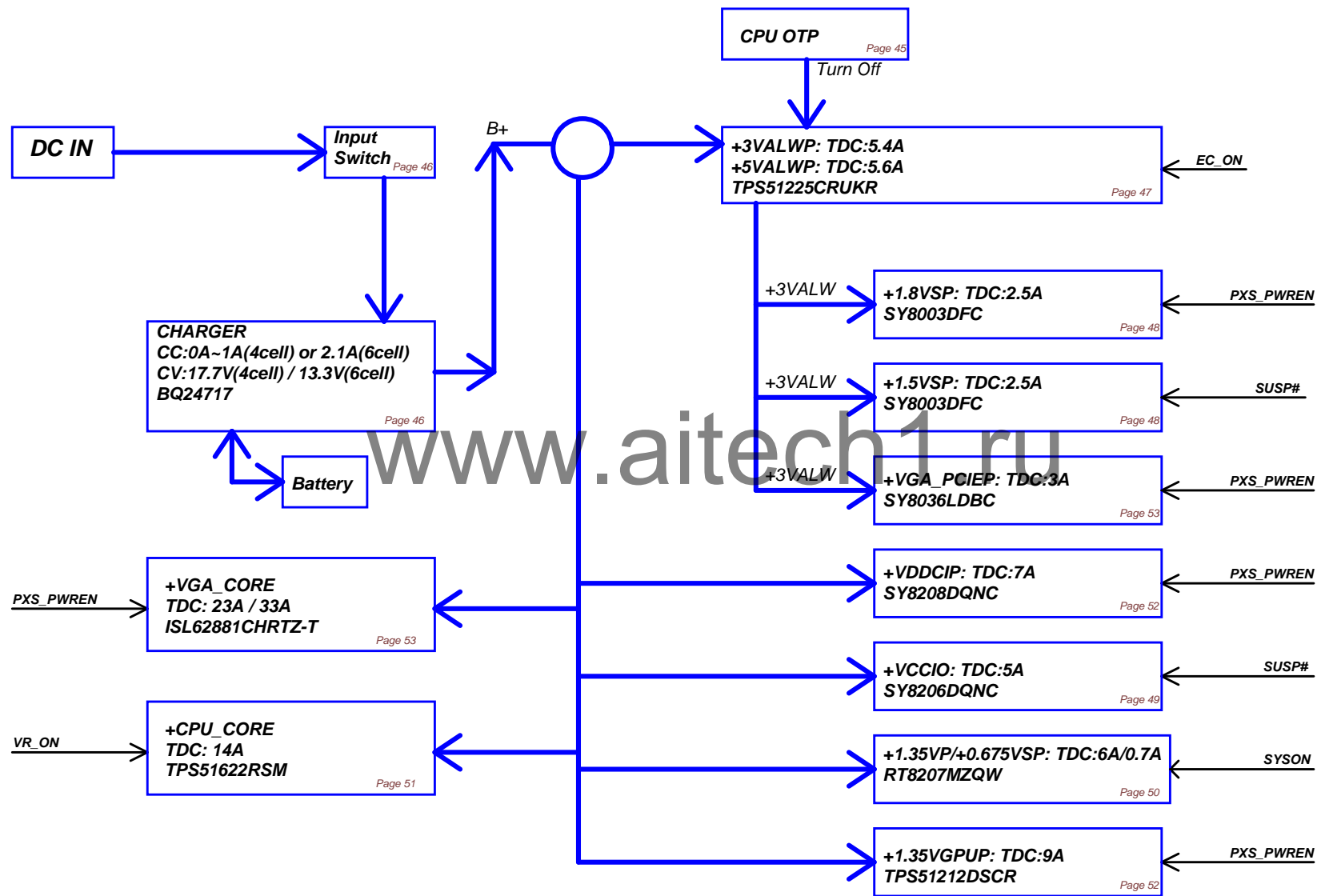
+VGA_CORE



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Power block



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				A	PWR-PIR	0.3
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